# Secondary Side Synchronous Rectifier (SR)

## FEATURES

- **Secondary Side Synchronous Rectifier(SR) for fly-back converters**
- **Supports High-Side and Low-Side in DCM and Quasi-Resonant Topologies**
- **<300uA Low Quiescent Current**
- **Built-in HV Supplies for VDD Capacitance to Eliminate Aux-Winding of VDD supply**
- **Built-in 15m Ω 50V Power MOSFET**
- **Built-in Protections:**
  - **VDD UVLO**
  - **VDD Clamper by >5mA sink current.**
- **SOP-7/SOP-8 package available**

## GENERAL DESCRIPTION

DP3520 is a secondary side synchronous rectifier, that replaced Schottky diodes by combined with an ultra low on-state resistance power MOSFET for high-efficiency fly-back converters. It supports High-Side and Low-Side in DCM and Quasi-Resonant Topologies.

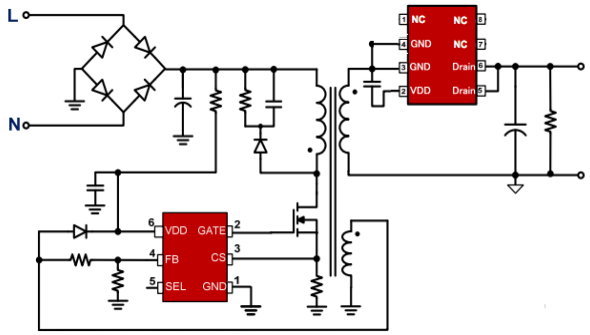
DP3520 is built-in HV supplies for VDD capacitance, that can eliminate the aux-winding of VDD supply for cost saving.

DP3520 integrates protections of Under Voltage Lockout (UVLO), VDD Clamper.

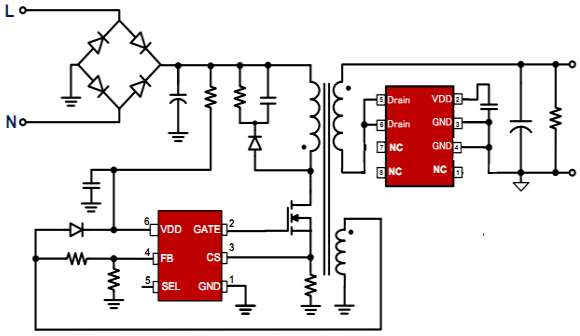
## APPLICATIONS

- **Flyback converters**
- **Adaptors**

## TYPICAL APPLICATION CIRCUIT

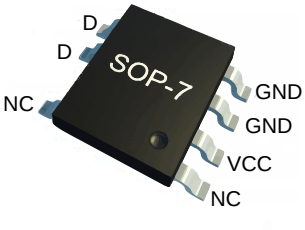



**High Side SR**

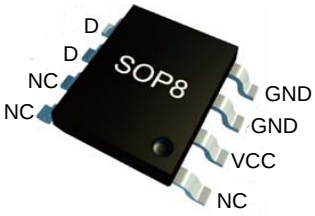



**Low Side SR**

## Pin Configuration




**SOP-7**




**SOP-8**

## Marking Information


**NOTE:**

**DPXXXX for product name;**

**XXXXXX The first X reresents the last year,2014 is 4; The second X represents the month, in A-L 12 letters;The third and fourth X on behalf of the date, 01-31 said; The last two X represents the wafer batch code.**

## Output Power Table

| Part Number | Package | BV for Internal MOSFET | System Operation Mode |
|---|---|---|---|
| DP3520 | SOP-7<br>SOP-8 | 50V | QR or DCM |

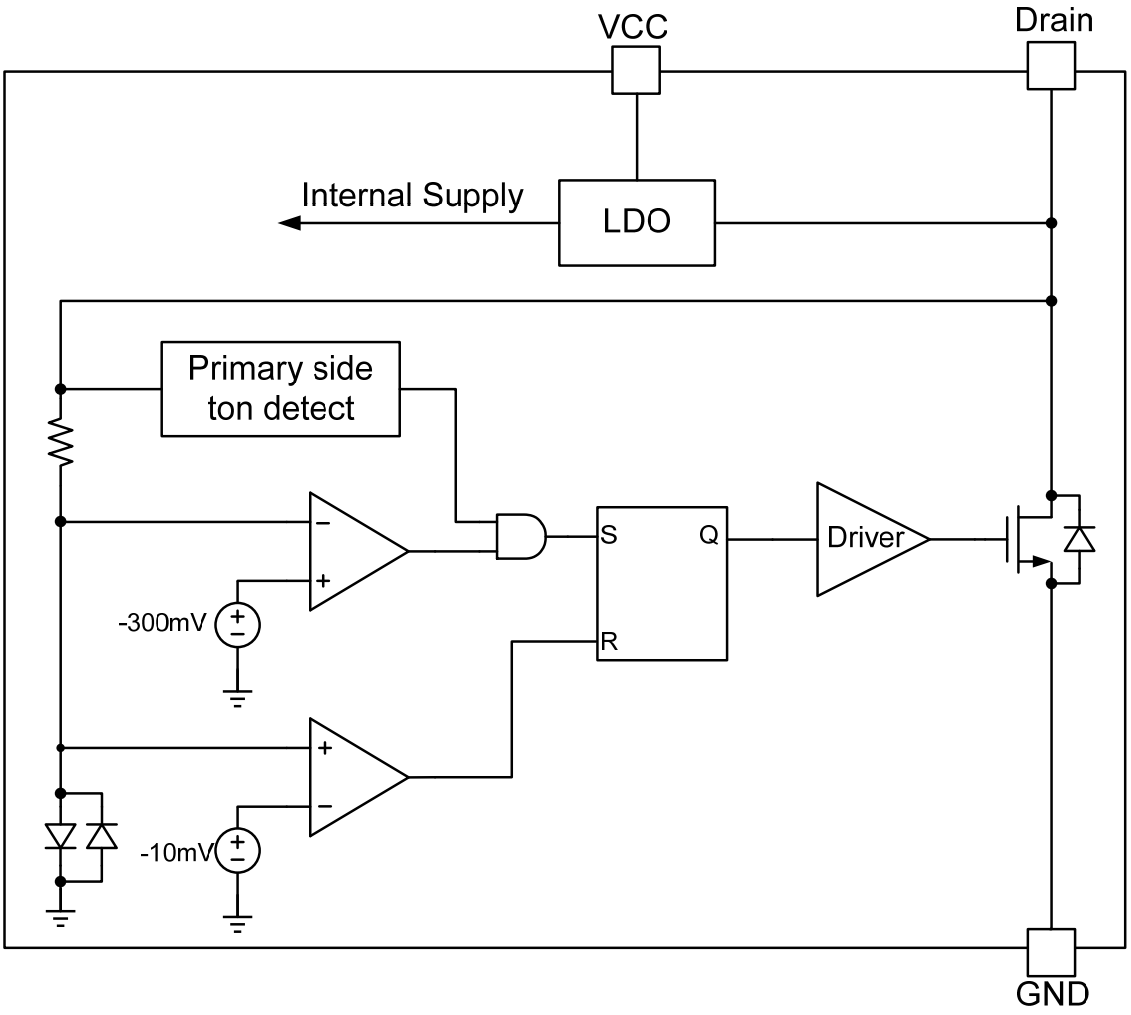
## Pin Description

| Pin Number | Pin Name | I/O | Description |
|---|---|---|---|
| 1,7,(8) | NC | --- | No Function Pin and Left Floating in Application |
| 2 | VCC | P | IC Power Supply Pin |
| 3,4 | GND | P | IC Ground Pin |
| 5,6 | D | I | Internal Power MOSFET Drain Pin |

## Ordering Information

| Part Number | Description |
|---|---|
| DP3520 | SOP-7/SOP-8,Halogen free in T&R,4000Pcs/Reel |

## Block Diagram



## Absolute Maximum Ratings (Note 1)

| Parameter | Value | Unit |
|---|---|---|
| Drain Pin Voltage Range | -0.3 to 50 | V |
| VDD DC Supply Voltage | 7 | V |
| VDD DC Clamp Current | 5 | mA |
| Package Thermal Resistance----Junction to Ambient | 165 | °C/W |
| Maximum Junction Temperature | 150 | °C |
| Storage Temperature Range | -65 to 150 | °C |
| Lead Temperature (Soldering, 10sec.) | 260 | °C |
| ESD Capability, HBM (Human Body Model) | 3 | kV |
| ESD Capability, MM (Machine Model) | 250 | V |

## Recommended Operation Conditions (Note 2)

| Parameter | Value | Unit |
|---|---|---|
| Operating Ambient Temperature | -40 to 125 | °C |

## Electrical Characteristics (Ta = 25°C, VDD=11V, if not otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage Section(VDD Pin)** | | | | | | |
| $I_Q$ | Quiescent Operation Current | VDD=6V,Drain=0V | 50 | 150 | 200 | uA |
| $V_{DD\_reg}$ | HV supply VDD regulation Voltage | Drain=12V | 5.7 | 6.1 | 6.5 | V |
| $I_{HV}$ | HV supply current | Drain=12V,VDD=5.5V | 15 | | 30 | mA |
| $V_{DD\_ON}$ | VDD Operation Voltage | VDD rising | 3.7 | 4 | 4.3 | V |
| $V_{DD\_OFF}$ | VDD Under Voltage Lockout Enter | VDD falling | 2.8 | 3.1 | 3.4 | V |
| $V_{DD\_Clamp}$ | VDD Zener Clamp Voltage | $I(V_{DD})$ = 5mA | | 7 | | V |
| **Internal MOSFET and Control Section(Drain Pin)** | | | | | | |
| Vth_off | Internal synchronous MOSFET turn off threshold voltage | | -15 | -10 | -5 | mV |
| Vth_on | Internal synchronous MOSFET turn on threshold | | | -300 | | mV |

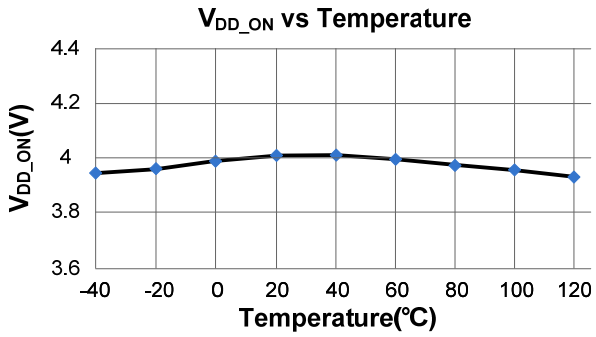
| | | | | | | |
|---|---|---|---|---|---|---|
| | voltage | | | | | |
| Rds_on | Internal synchronous MOSFET on-state resistance | VDD=5.5V，Id=6A | | 15 | 20 | mΩ |
| Td_on | Internal synchronous MOSFET turn on delay time | | | | 200 | ns |
| Td_off | Internal synchronous MOSFET turn off delay time | | | | 60 | ns |
| $V_{BR}$ | Internal synchronous MOSFET Drain Source Breakdown Voltage | | 45 | 50 | | V |

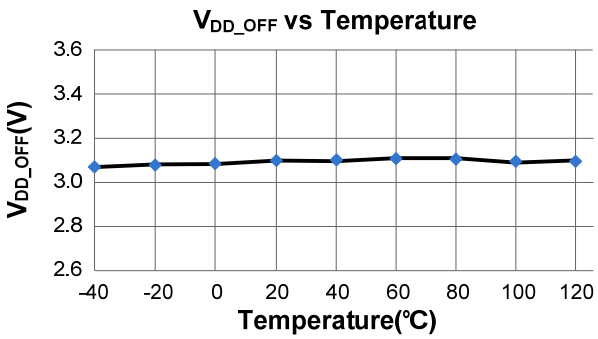
**Note 1.** Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** The device is not guaranteed to function outside its operating conditions.

**Note 3.** Guaranteed by the Design.

## Characterization Plots



## Operation Description

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### ● 6.1V Regulator

In DP3520, the 6.1V regulator charges VDD hold-up capacitor to 6.1V by drawing a current from the voltage on the Drain pin during the on state of primary side. A capacitor value about 1uF is sufficient for both high frequency decoupling and energy storage.

### ● System Start-Up Operation

After system power up, VDD hold up capacitor is charged by the internal LDO through Drain pin.

When VDD pin voltage is below UVLO threshold (3V), the IC is in sleep mode and the internal synchronous MOSFET is keeping off. The current flows through body diode of the internal synchronous MOSFET. When VDD pin voltage reaches the turn on threshold, the IC begins working. The internal synchronous MOSFET can be only turned on during the demagnetization time of the transformer.

### ● Turn-on Phase

When the internal synchronous MOSFET is off, current will flow through its body diode which can generate a negative Vds(<-500mV) across it. The body diode drop voltage Vds is much smaller than the turn on threshold of DP3520 (-300mV), which will turn on the internal synchronous MOSFET after about 200ns turn on delay (Td_on). (Shown in Fig 1)

### ● Turn-off Phase

During the turn-on period of the internal synchronous MOSFET, The DP3520 senses the drop voltage Vds across the on-state resistance of the MOSFET. When Vds is higher than the turn off threshold (-10mV typically), the internal synchronous MOSFET will be turned off after about 60ns turn on delay (Td_off). (Shown in Fig 1)

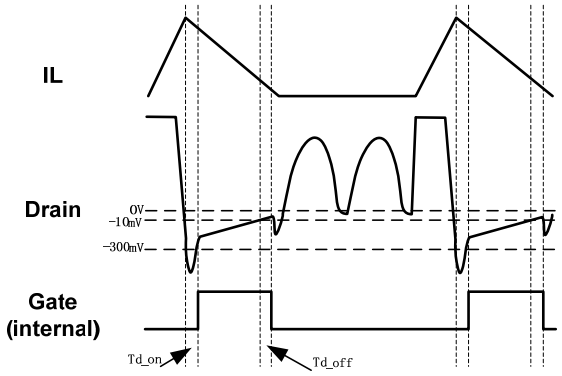


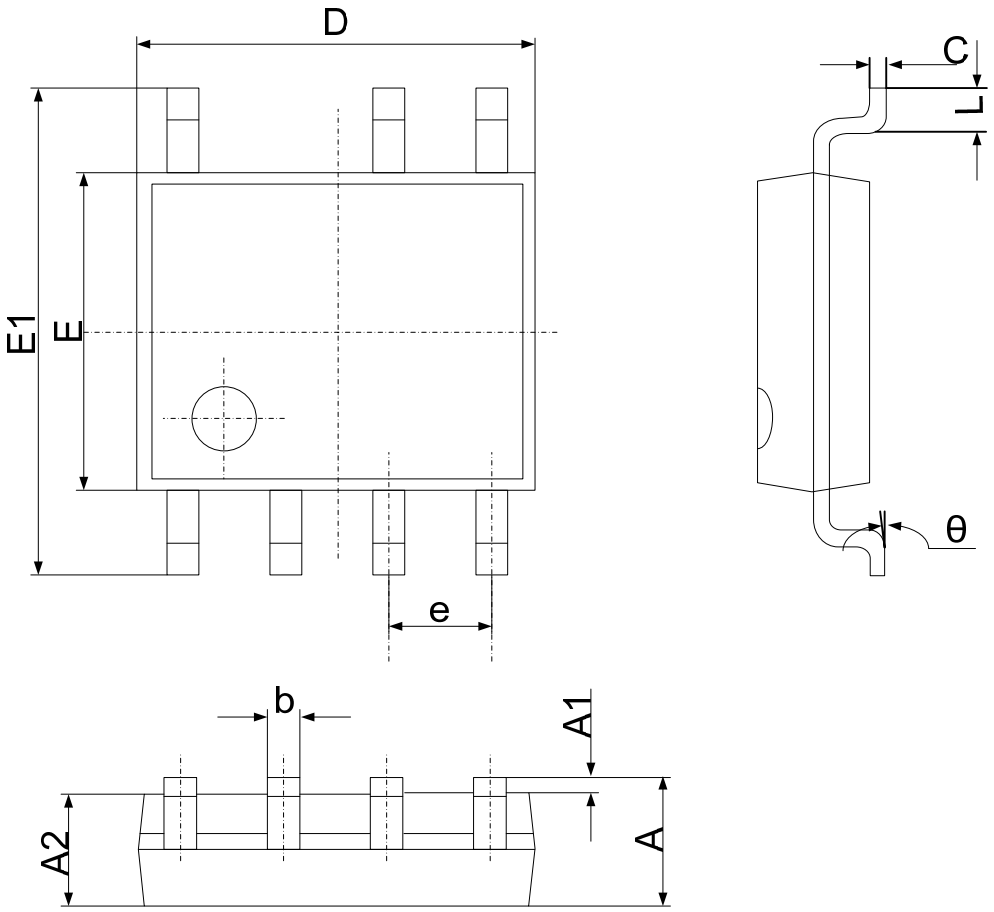

Fig 1

### ● Leading Edge Blanking (LEB)

Each time the internal synchronous MOSFET is switched on, a turn-on spike occurs across the Drain and GND. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (1us, typical), the turn-off comparator is disabled and cannot switch off the internal synchronous MOSFET.

## Package Dimension

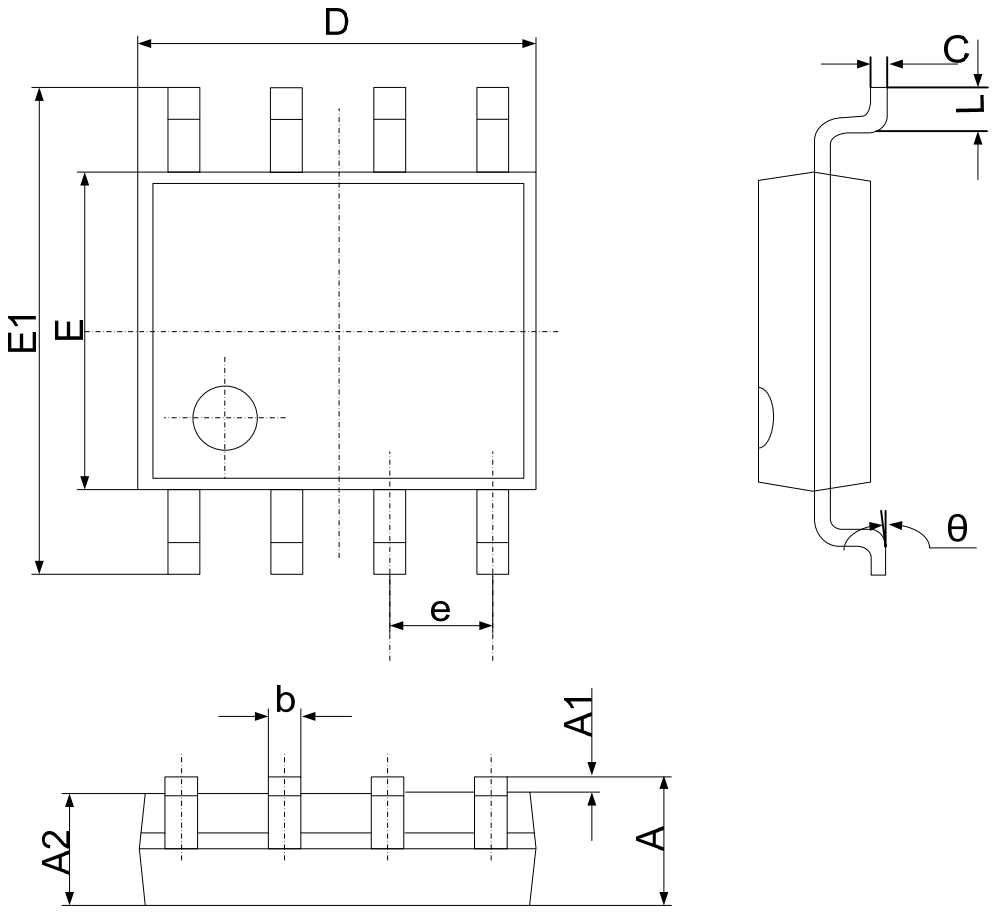
**SOP-7**




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

## Package Dimension

**SOP-8**




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
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| | Min | Max | Min | Max |
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| θ | 0° | 8° | 0° | 8° |