QUALCOMM® QUICK CHARGE™ 3.0 TECHNOLOGY

VERIFICATION TEST REPORT

FOR

IC

MODEL NUMBER: FP6601Q

REPORT NUMBER: 4787452994-1

ISSUE DATE: August 12, 2016

Prepared for
FITIPOWER INTEGRATED TECHNOLOGY INC
3RD FL, 6-8, DUXING RD., HSINCHU SCIENCE PARK, HSINCHU 300, TAIWAN

Prepared by
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Revision History

Rev.	Issue Date	Revisions	Revised By
--	2016/8/12	Initial Issue	J.Hu

TABLE OF CONTENTS

1. ATTESTATION OF TEST RESULTS

COMPANY NAME: FITIPOWER INTEGRATED TECHNOLOGY INC
3RD FL, 6-8, DUXING RD., HSINCHU SCIENCE PARK,
HSINCHU 300, TAIWAN

EUT DESCRIPTION: IC

MODEL: FP6601Q

SERIAL NUMBER: Prototype

DATE TESTED: August 10, 2016

APPLICABLE STANDARDS	
STANDARD	TEST RESULTS
High Voltage Dedicated Charging Port Interface Specification Revision J	Pass

UL Taiwan Co., Ltd. tested the above equipment in accordance with the requirements set forth in the above standards. All indications of Pass/Fail in this report are opinions expressed by UL Taiwan Co., Ltd. based on interpretations and/or observations of test results. Measurement Uncertainties were not taken into account and are published for informational purposes only. The test results show that the equipment tested is capable of demonstrating compliance with the requirements as documented in this report.

Note: The results documented in this report apply only to the tested sample, under the conditions and modes of operation as described herein. This document may not be altered or revised in any way unless done so by UL Taiwan Co., Ltd. and all revisions are duly noted in the revisions section. Any alteration of this document not carried out by UL Taiwan Co., Ltd. will constitute fraud and shall nullify the document. This report must not be used by the client to claim product certification, approval, or endorsement by Qualcomm.

Approved & Released For
UL Taiwan Co. Ltd. By: Tested By:

James Hu   _Daniel Chiang_

_____   _____

James Hu   Daniel Chiang
PROJECT ENGINEER   PROJECT ENGINEER
UL Taiwan Co. Ltd.   UL Taiwan Co., Ltd

2. TRADEMARK NOTICES

Qualcomm is a trademark of Qualcomm Incorporated, registered in the United States and other countries. Qualcomm Quick Charge is a trademark of Qualcomm Incorporated. All Qualcomm Incorporated marks are used with permission.

3. TEST METHODOLOGY

The tests documented in this report were performed in accordance with High Voltage Dedicated Charging Port HVDCP Compliance Plan Revision D as amended by instructions from Qualcomm.

4. FACILITIES AND ACCREDITATION

The test sites and measurement facilities used to collect data are located at 5th Fl., 35, Sec. 2, Chungyang S. Road, Peitou District, Taipei City, Taiwan 112.

UL Taiwan Co., Ltd. is accredited by Taiwan Accreditation Foundation (TAF), Laboratory Code 0944. The full scope of accreditation can be viewed at http://hr.taftw.org.tw/service/labinfoE.aspx?code=0944.

Notes:
1. All measurements documented in this report are outside the scope of the Laboratory's TAF accreditation.
2. The Laboratory used for performing the measurements documented in this report is third party accredited to ISO 17025.

5. CALIBRATION AND UNCERTAINTY

5.1. MEASURING INSTRUMENT CALIBRATION

The measuring equipment utilized to perform the tests documented in this report has been calibrated in accordance with the manufacturer's recommendations, and is traceable to recognized national standards.

5.2. TEST AND MEASUREMENT EQUIPMENT

The following test and measurement equipment was utilized for the tests documented in this report:

TEST EQUIPMENT LIST					
Description	Manufacturer	Model	Asset	Cal Date	Cal Due
Current Probe	LeCroy	CP030	135753	2016/3/24	2017/3/31
SourceMeter SMU instrument	KEITHLEY	2606B	85188	2016/6/8	2017/6/30
Oscilloscope	LeCroy	HDO6034	85085	2016/6/8	2017/6/30
Electronic Load	Prodigit	3311F / 3305F	74130	2015/11/23	2016/11/30
Multimeter	Yokogawa	TY720	87025	2015/10/29	2016/10/31

6. EQUIPMENT UNDER TEST

6.1.   DESCRIPTION OF EUT

The EUT is a QUALCOMM® Quick Charge™ 3.0 Class A charger.

It is a chipset module reference design.

Input power is furnished by a 18V DC power source. (5A max, for reference)

The rated output current at each output voltage is as follows:

Output Voltage (Volts)	Rated Current (Amps)
5	3
9	3
12	3

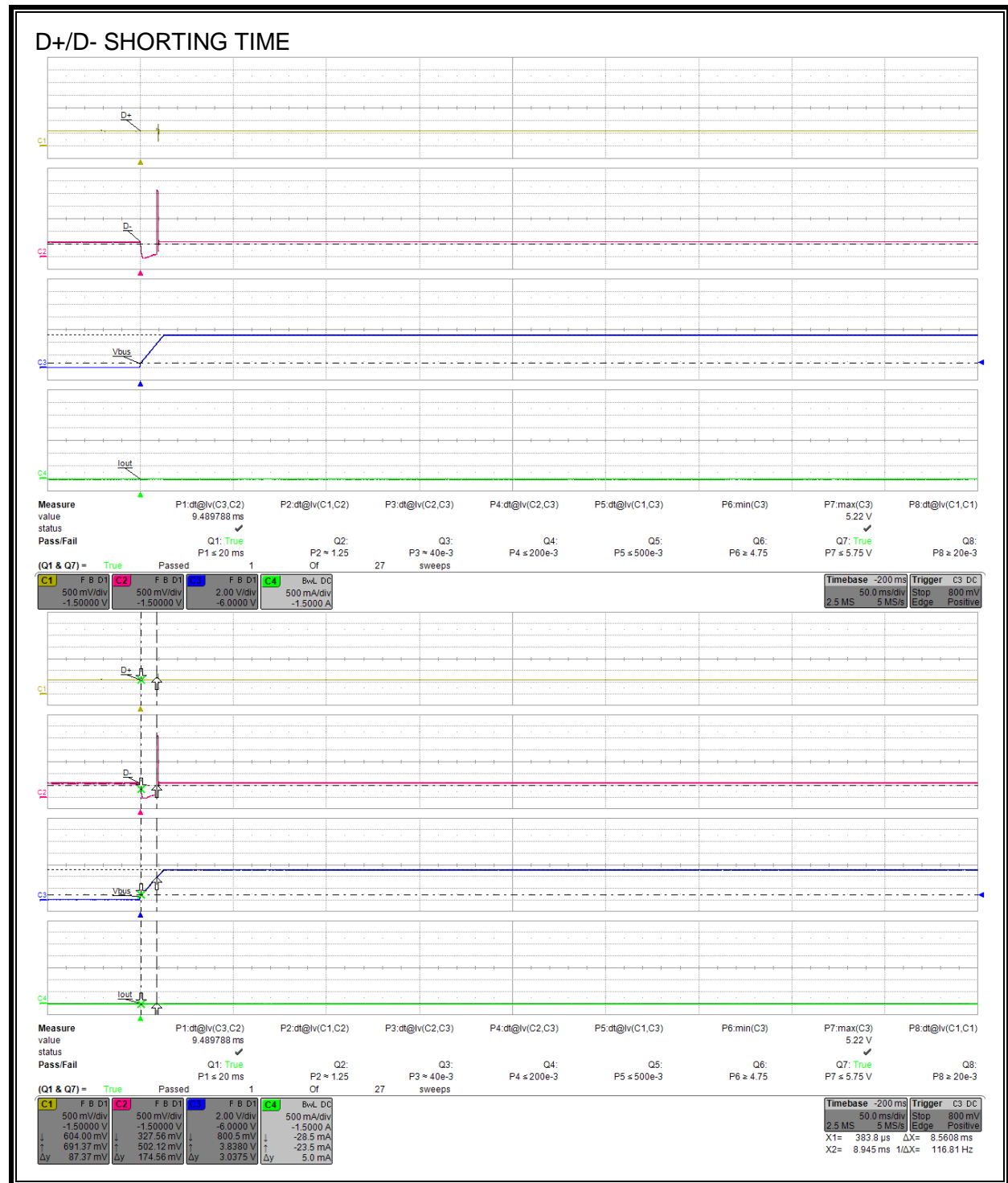The Quick Charge output is furnished via a USB Type A connector.

7. TEST RESULTS

7.1.   HVDCP Insertion

7.1.1. D+/D- Shorting Time

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (ms)	Maximum Limit (ms)	Pass/Fail
Td+_d-_short	Vbus >= 0.8 V (Min Votg_sess_vld)	D- >= 0.5 V (Min Vdm_src)	8.560	20	PASS

WAVEFORM AND MEASUREMENTS

D+/D- SHORTING TIME

Measure	P1:dt@lv(C3,C2)	P2:dt@lv(C1,C2)	P3:dt@lv(C2,C3)	P4:dt@lv(C2,C3)	P5:dt@lv(C1,C3)	P6:min(C3)	P7:max(C3)	P8:dt@lv(C1,C1)
value	9.489788 ms						5.22 V	
status	✓						✓	
Pass/Fail	Q1: True	Q2:	Q3:	Q4:	Q5:	Q6:	Q7: True	Q8:
	P1 ≤ 20 ms	P2 ≈ 1.25	P3 ≈ 40e-3	P4 ≤ 200e-3	P5 ≤ 500e-3	P6 ≥ 4.75	P7 ≤ 5.75 V	P8 ≥ 20e-3

(Q1 & Q7) = True   Passed   1   Of   27   sweeps

C1	F B D1	C2	F B D1	C3	F B D1	C4	BwL DC
500 mV/div		500 mV/div		2.00 V/div		500 mA/div	
-1.50000 V		-1.50000 V		-6.0000 V		-1.5000 A	

Timebase -200 ms Trigger C3 DC
50.0 ms/div Stop 800 mV
2.5 MS 5 MS/s Edge Positive

Measure	P1:dt@lv(C3,C2)	P2:dt@lv(C1,C2)	P3:dt@lv(C2,C3)	P4:dt@lv(C2,C3)	P5:dt@lv(C1,C3)	P6:min(C3)	P7:max(C3)	P8:dt@lv(C1,C1)
value	9.489788 ms						5.22 V	
status	✓						✓	
Pass/Fail	Q1: True	Q2:	Q3:	Q4:	Q5:	Q6:	Q7: True	Q8:
	P1 ≤ 20 ms	P2 ≈ 1.25	P3 ≈ 40e-3	P4 ≤ 200e-3	P5 ≤ 500e-3	P6 ≥ 4.75	P7 ≤ 5.75 V	P8 ≥ 20e-3

(Q1 & Q7) = True   Passed   1   Of   27   sweeps

C1	F B D1	C2	F B D1	C3		C4	BwL DC
500 mV/div		500 mV/div		2.00 V/div		500 mA/div	
-1.50000 V		-1.50000 V		-6.0000 V		-1.5000 A	
604.00 mV		327.56 mV		800.5 mV		-28.5 mA	
691.37 mV		502.12 mV		3.8380 V		-23.5 mA	
Δy 87.37 mV		Δy 174.56 mV		Δy 3.0375 V		Δy 5.0 mA	

Timebase -200 ms Trigger C3 DC
50.0 ms/div Stop 800 mV
2.5 MS 5 MS/s Edge Positive
X1= 383.8 µs ΔX= 8.5608 ms
X2= 8.945 ms 1/ΔX= 116.81 Hz

7.1.2. D+/D- Remains Shorted at 3.3 V

LIMITS AND RESULTS
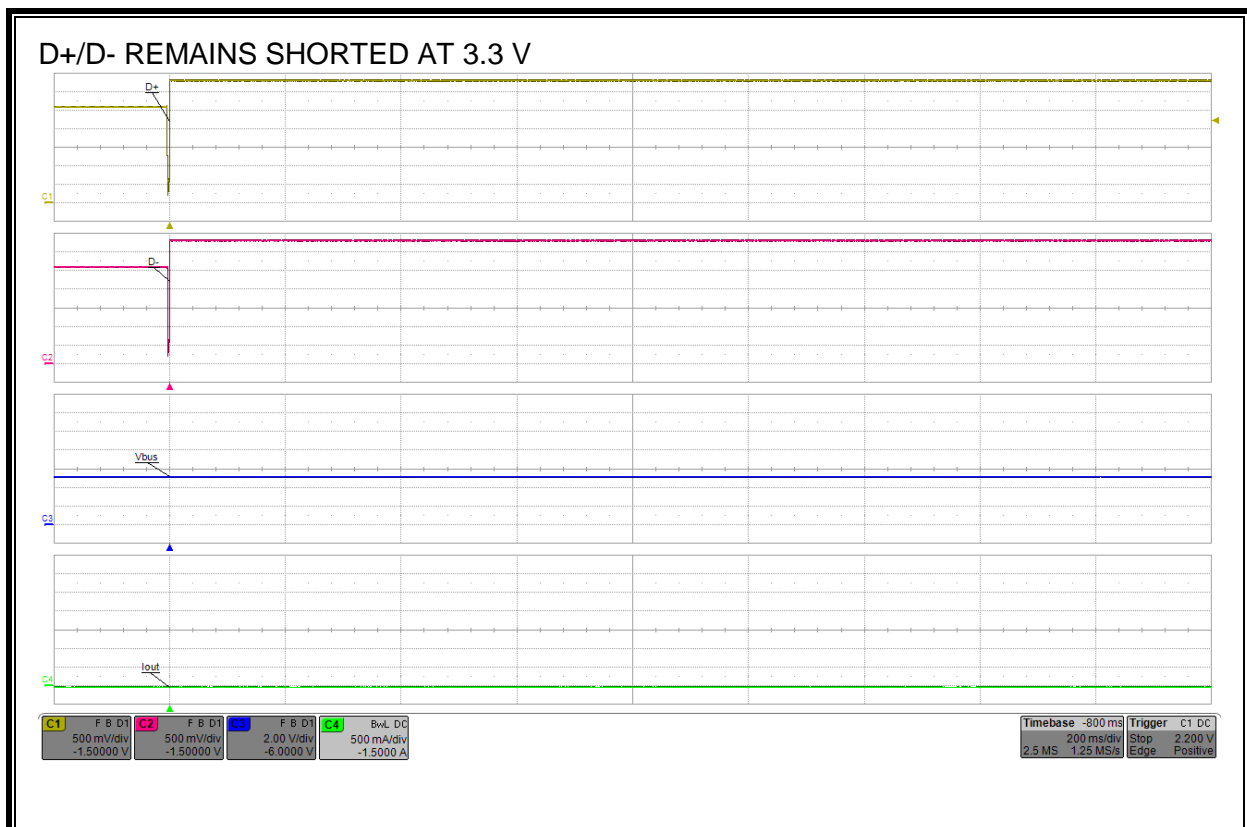
Requirement: D- remains shorted to D+ when D+ is set to 3.3 V and D- Floats

Beginning 1.5 seconds (Max Tglitch_bc_done) after D+ >= 2.2 V (Max Vsel_ref),
confirm D- >= 2.2 V (Max Vsel_ref)

Parameter	Measured Value (V)	Minimum Limit (V)	Pass/Fail
D-	3.30	2.2	PASS

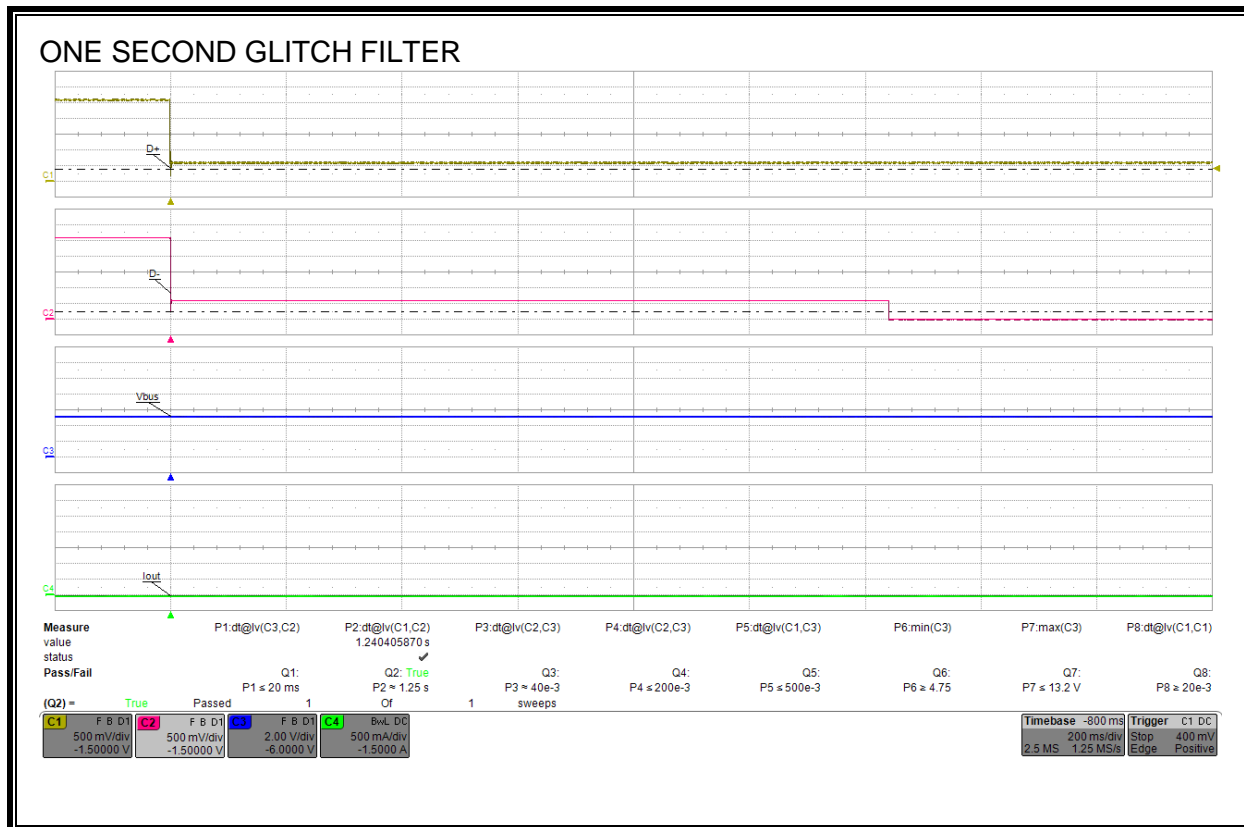**WAVEFORM AND MEASUREMENTS**

7.2.   HVDCP Negotiation

7.2.1. One Second Glitch Filter

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (s)	Minimum Limit (s)	Maximum Limit (s)	Pass/Fail
Tglitch_bc_done	D+ >= 0.4 V (Max Vdat_ref)	D- <= 0.25 V (Min Vdat_ref)	1.24	1.0	1.5	PASS

WAVEFORM AND MEASUREMENTS

7.2.2. Rdcp_dat

LIMITS AND RESULTS

Measured D+ Voltage (V)	Measured D- Voltage (V)	Measured D+ Current (mA)	Rdcp_dat Measured Value (ohms)	Rdcp_dat Maximum Limit (ohms)	Pass/Fail
0.600	0.593	0.984	7.3	40	PASS

7.2.3. Rdm_dwn

LIMITS AND RESULTS

Parameter	Measured Value (k ohms)	Minimum Limit (k ohms)	Maximum Limit (k ohms)	Pass/Fail
Rdm_dwn	20.910	14.25	24.80	PASS

7.2.4. Rdat_lkg

LIMITS AND RESULTS

Parameter	Measured Value (k ohms)	Minimum Limit (k ohms)	Maximum Limit (k ohms)	Pass/Fail
Rdat_lkg	823.3	300	1500	PASS

7.3. PD Request Recognition

7.3.1. Output Voltage

LIMITS AND RESULTS

Output Voltage at No Load					
Nominal Vbus (V)	Load Current (A)	Measured Vbus (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
5	0.0	5.13	4.75	5.50	PASS
9	0.0	9.26	8.10	9.90	PASS
12	0.0	12.36	10.80	13.20	PASS

Output Voltage at Max Rated Load				
Nominal Vbus (V)	Load Current (A)	Measured Vbus (V)	Minimum Limit (V)	Pass/Fail
5	3.00	4.98	4.75	PASS
9	3.00	9.13	8.10	PASS
12	3.00	12.25	10.80	PASS

7.3.2. Transition from 5 V to 12 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 5.5 V (Max Vbus_5v)	39.79	20	60	PASS
Tv_new_request	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 10.8 V (Min Vbus_hv)	40.63		200	PASS

WAVEFORM AND MEASUREMENTS
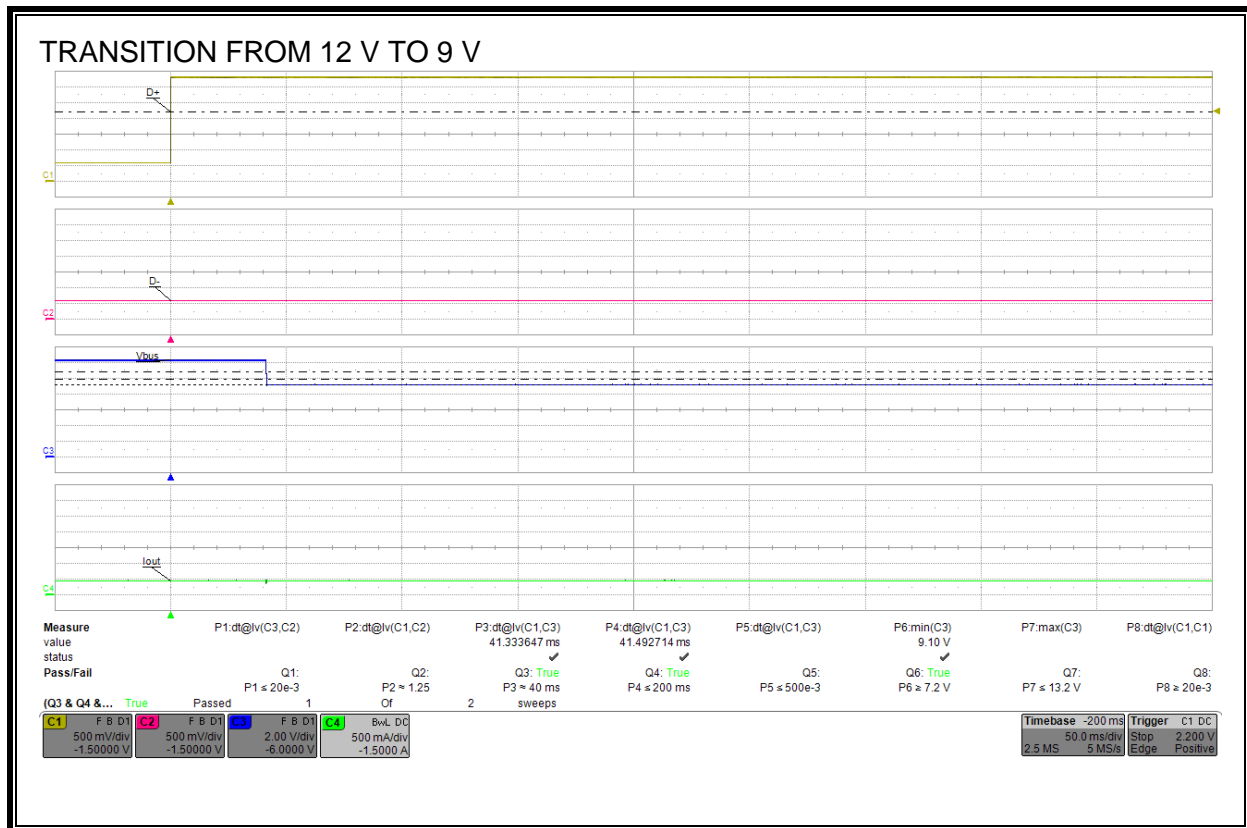

TRANSITION FROM 5 V TO 12 V
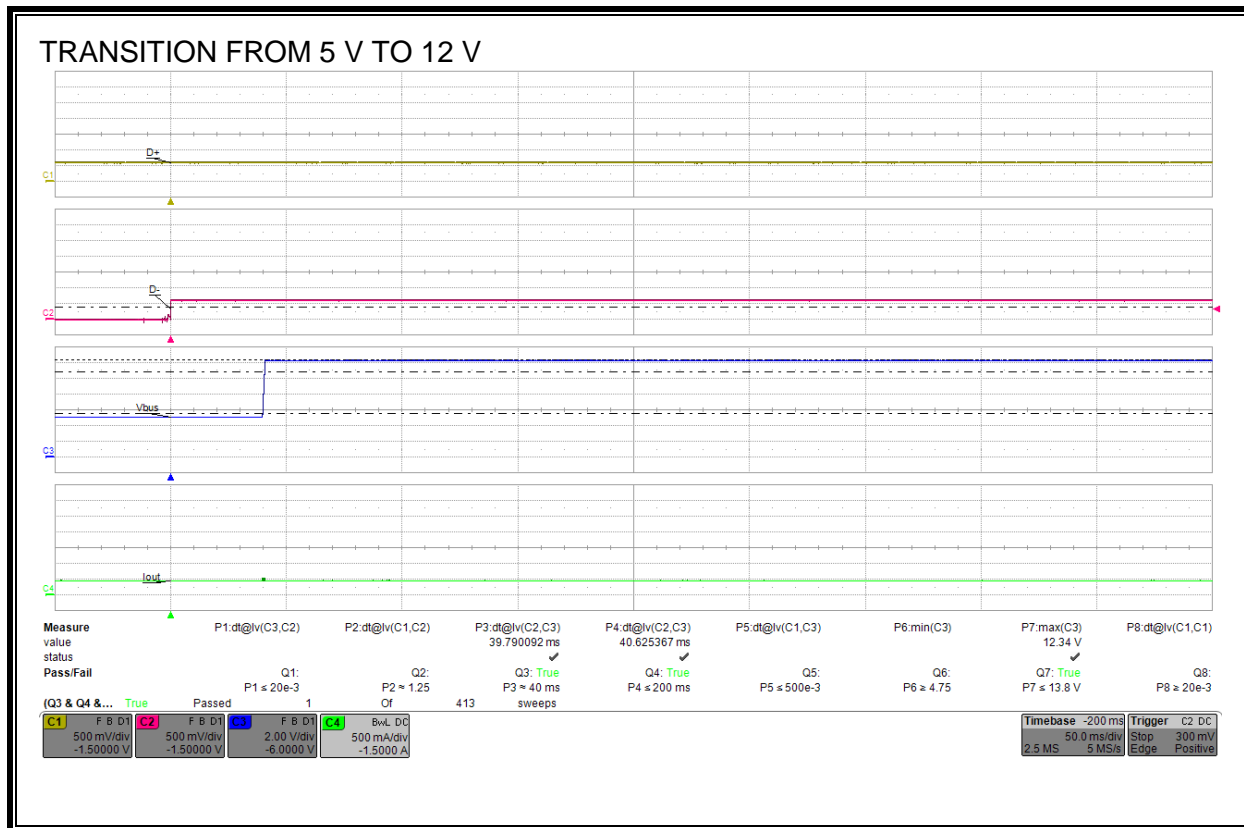
7.3.3. Transition from 12 V to 9 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 10.8 V (Min Vbus_hv)	41.33	20	60	PASS
Tv_new_request	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 9.9 V (Max Vbus_hv)	41.49		200	PASS

WAVEFORM AND MEASUREMENTS

7.3.4. Maintain 9 V with 20 V Request

LIMITS AND RESULTS

Initial Condition: Vbus is 9 volts

Observation Period: Monitor for longer than 200 ms (Max Tv_new_request) after 20 Volt Request is asserted

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	9.200	8.10	9.90	PASS

WAVEFORM AND MEASUREMENTS

MAINTAIN 9 V WITH 20 V REQUEST

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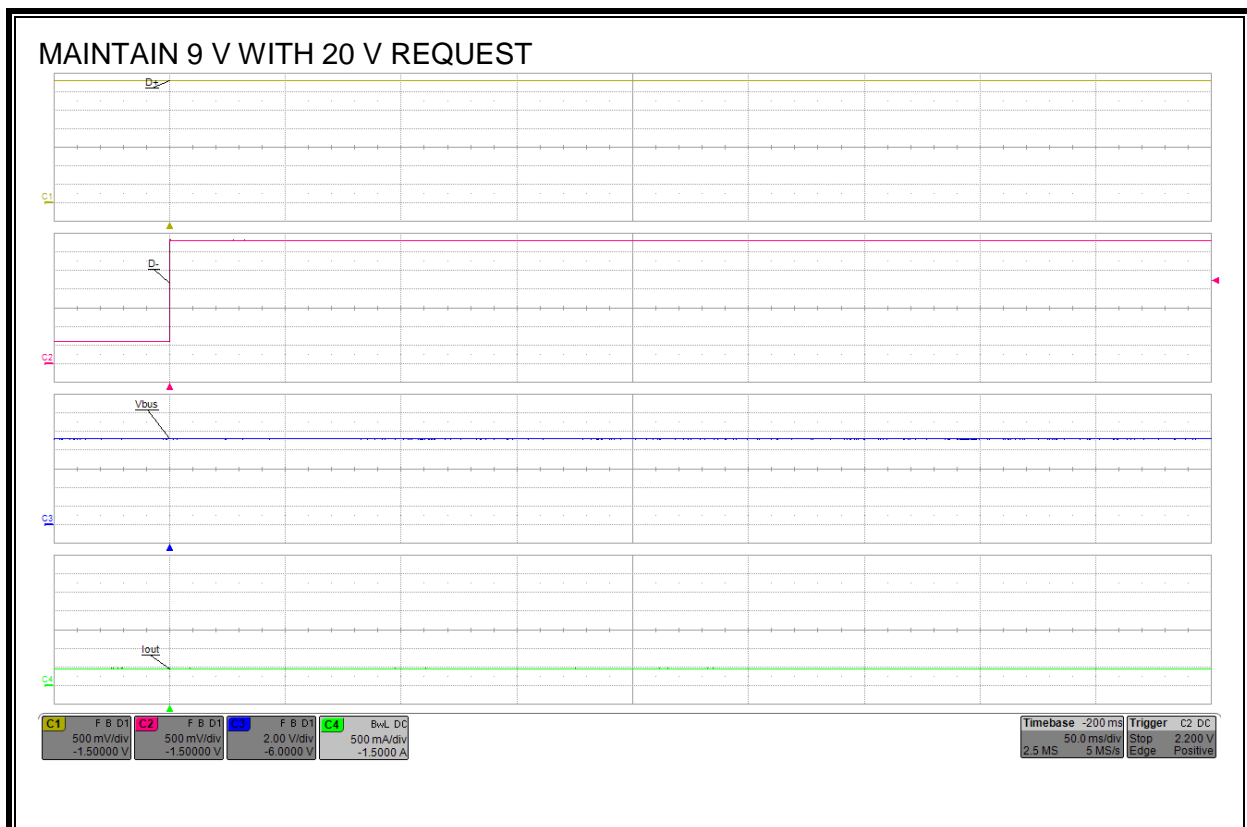
7.3.5. Maintain 9 V with Continuous Request

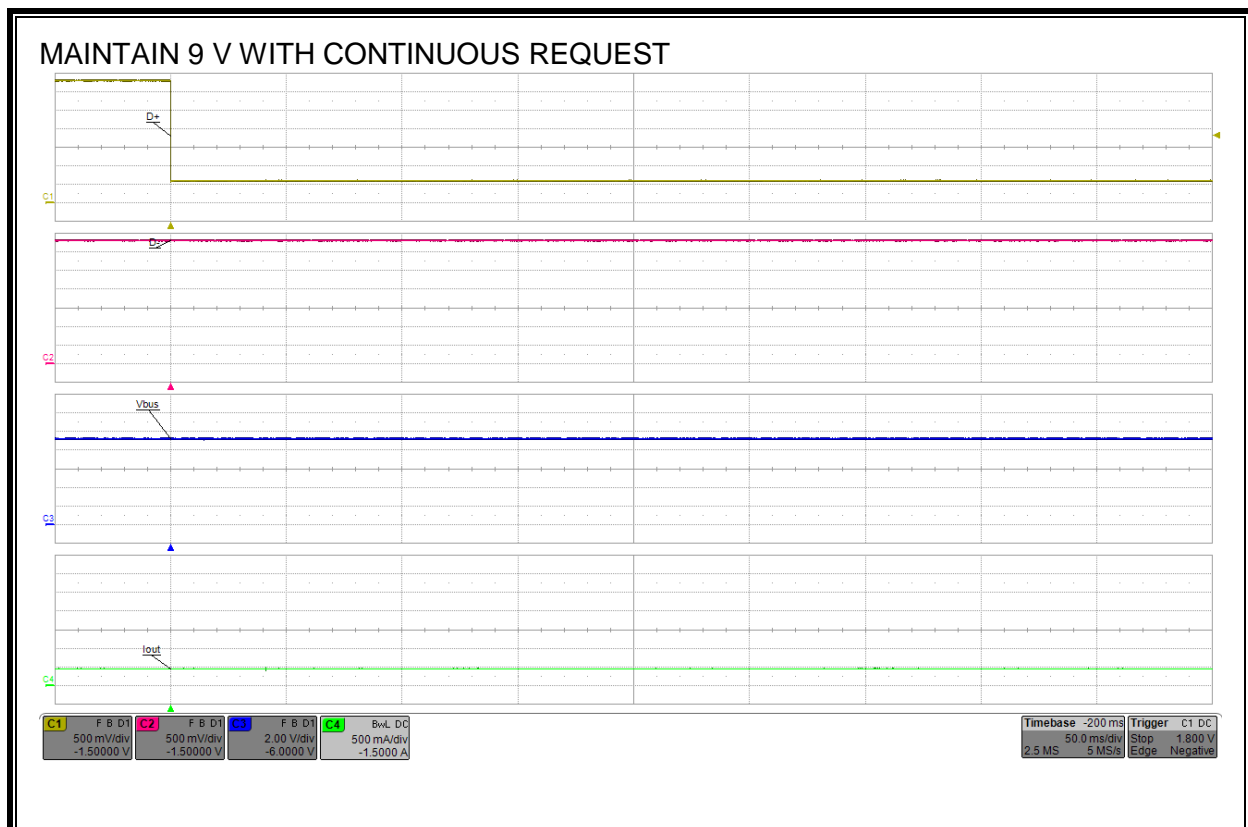**LIMITS AND RESULTS**

Initial Condition: Vbus is 9 volts

Observation Period: Monitor for longer than 200 ms (Max Tv_new_request) after Continuous Request is asserted

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	9.200	8.10	9.90	PASS

WAVEFORM AND MEASUREMENTS

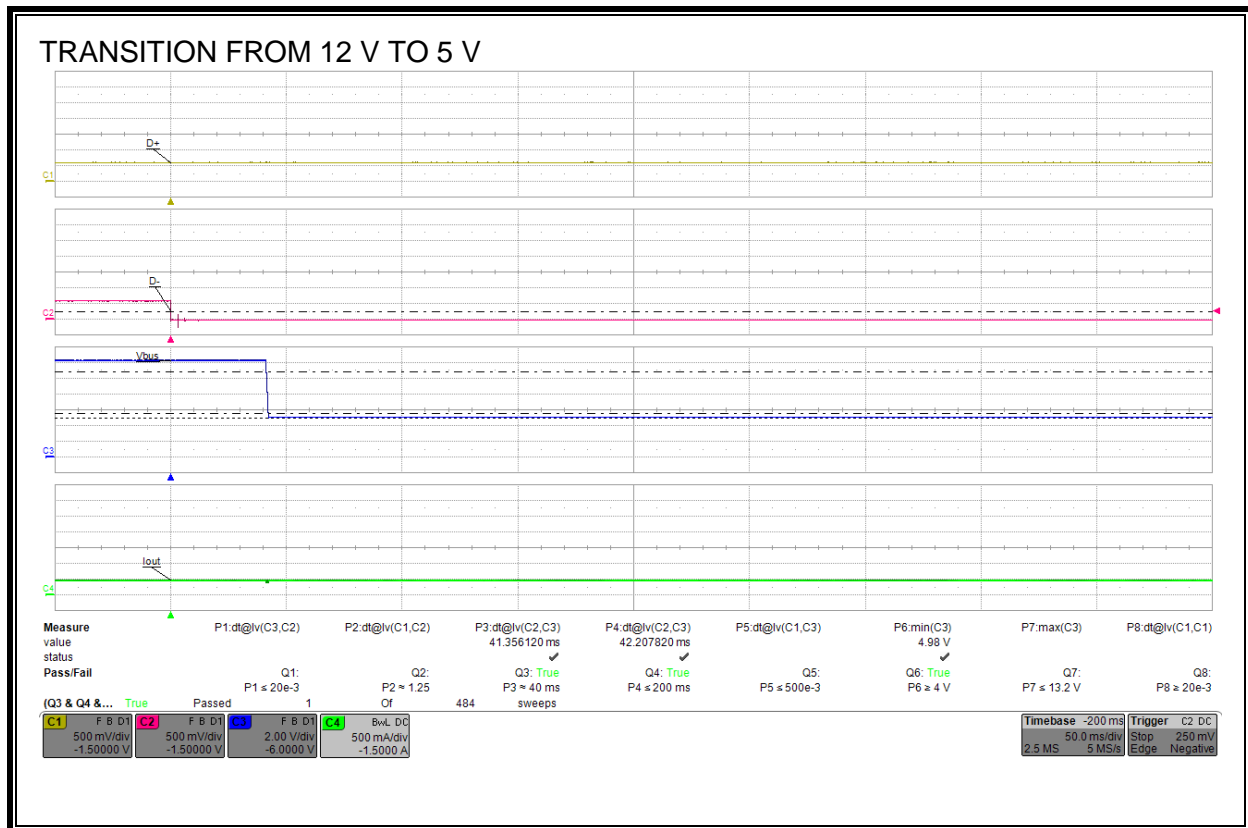
MAINTAIN 9 V WITH CONTINUOUS REQUEST

7.3.6. Transition from 12 V to 5 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 10.8 V (Min Vbus_hv)	41.36	20	60	PASS
Tv_new_request	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 5.5 V (Max Vbus_5v)	42.21		200	PASS

WAVEFORM AND MEASUREMENTS

7.4.   PD Removal

7.4.1. Unplug Vbus Discharge Time

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (ms)	Maximum Limit (ms)	Pass/Fail
Tv_unplug	D+ <= 0.5 V (Min Vdp_src)	Vbus <= 5.5 V (Max Vbus_5v)	2.87	500	PASS

Note: Confirm that Vbus go below 4.75V for 13.239ms.
          Hand operated of unplug directly for testing.

WAVEFORM AND MEASUREMENTS

UNPLUG VBUS DISCHARGE TIME

Measure	P1:dt@lv(C3,C2)	P2:dt@lv(C1,C2)	P3:dt@lv(C2,C3)	P4:dt@lv(C2,C3)	P5:dt@lv(C1,C3)	P6:min(C3)	P7:max(C3)	P8:dt@lv(C1,C1)
value					2.866492 ms	4.37 V		
status								
Pass/Fail	Q1:	Q2:	Q3:	Q4:	Q5: True	Q6:	Q7:	Q8:
	P1 ≤ 20e-3	P2 ≈ 1.25	P3 ≈ 40e-3	P4 ≤ 200e-3	P5 ≤ 500 ms	P6 ≥ 4 V	P7 ≤ 13.2	P8 ≥ 20e-3
(Q5) = True	Passed	1	Of	49	sweeps			

C1	F B D1	C2	F B D1	C3	F B D1	C4	BwL DC		Timebase -800 ms	Trigger C1 DC
500 mV/div		500 mV/div		2.00 V/div		500 mA/div			200 ms/div	Stop 500 mV
-1.50000 V		-1.50000 V		-6.0000 V		-1.5000 A			2.5 MS 1.25 MS/s	Edge Negative

Measure	P1:dt@lv(C3,C2)	P2:dt@lv(C1,C2)	P3:dt@lv(C2,C3)	P4:dt@lv(C2,C3)	P5:dt@lv(C1,C3)	P6:min(C3)	P7:max(C3)	P8:dt@lv(C1,C1)
value					2.866492 ms	4.37 V		
status								
Pass/Fail	Q1:	Q2:	Q3:	Q4:	Q5: True	Q6:	Q7:	Q8:
	P1 ≤ 20e-3	P2 ≈ 1.25	P3 ≈ 40e-3	P4 ≤ 200e-3	P5 ≤ 500 ms	P6 ≥ 4 V	P7 ≤ 13.2	P8 ≥ 20e-3
(Q5) = True	Passed	1	Of	49	sweeps			

C1	F B D1	C2	F B D1	C3	F B D1	C4	BwL DC	Z1	zoom(C3)		Timebase -800 ms	Trigger C1 DC
500 mV/div		500 mV/div		2.00 V/div		500 mA/div			500 mV/div		200 ms/div	Stop 500 mV
-1.50000 V		-1.50000 V		-6.0000 V		-1.5000 A			5.00 ms/div		2.5 MS 1.25 MS/s	Edge Negative
↓ 2.66281 V		↓ 2.65506 V		↑ 4.7497 V		↓ -19.9 mA			4.7497 V		X1= 227.877 ms	ΔX= 13.239 ms
↑ 2.66481 V		↑ 2.66144 V		↑ 4.7497 V		↑ -17.0 mA			4.7497 V		X2= 241.116 ms	1/ΔX= 75.533 Hz
Δy 2.00 mV		Δy 6.37 mV		Δy 0.0 mV		Δy 2.9 mA			0.0 mV			

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7.5. PD USB PHY Error Rejection

7.5.1. Square Wave Error Rejection

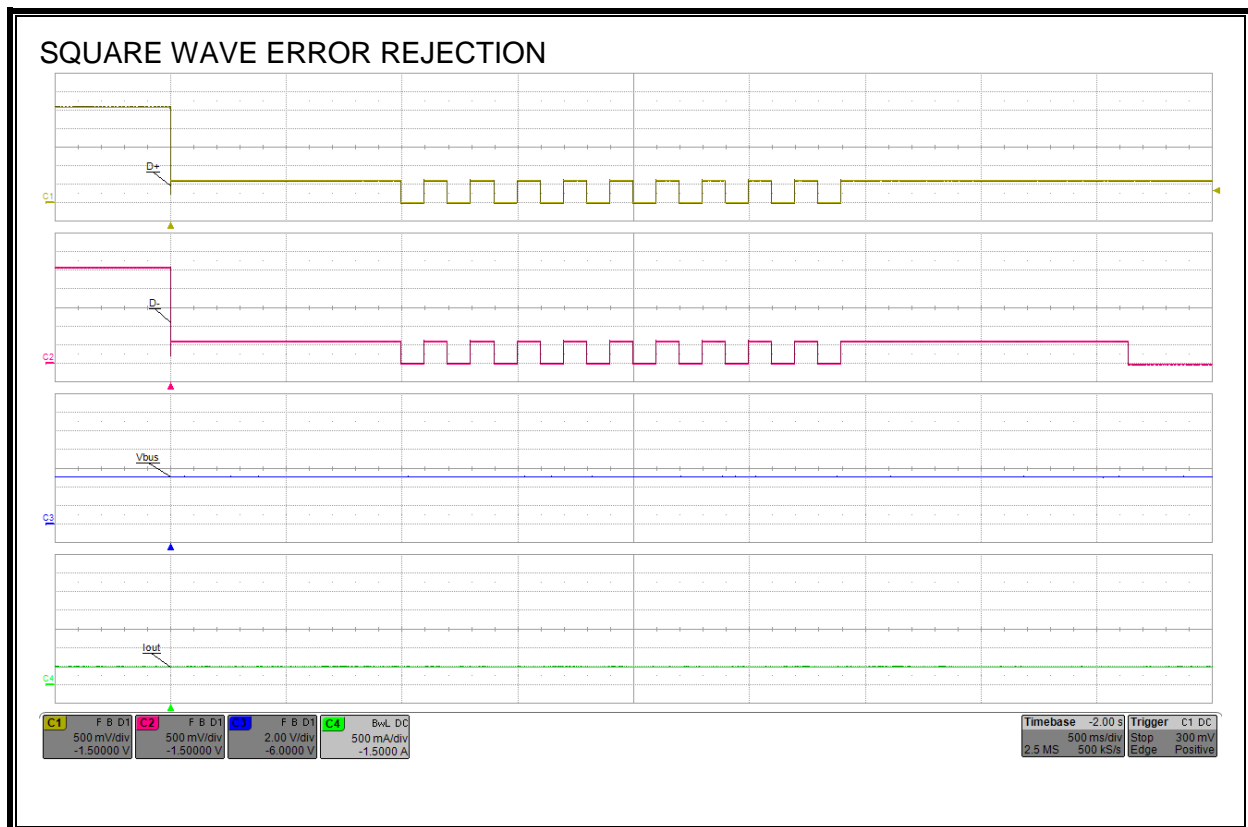**LIMITS AND RESULTS**

Initial Condition: Vbus is 5 volts
Applied Waveform: D+ = 0.6 V for 990 ms, then 0.6 V / 0 V pulse train, then remains at 0.6 V
Requirements: D- tracks D+ until Tglitch_bc_done after the completion of the pulse train, and Vbus remains at 5 volts
Observation Period: Monitor until at least 1.5 seconds after pulse train

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
D+/ D- Tracking				PASS
Vbus	5.103	4.75	5.50	PASS

WAVEFORM AND MEASUREMENTS

7.5.2. D+/D- External Short Error Rejection

LIMITS AND RESULTS

Initial Condition: Vbus is 5 volts
Applied Waveform: D+ and D- externally shorted together and held at 0 volts
Then 0.6 volts is applied to D+/D-
Requirement: Vbus remains at 5 volts
Observation Period: Monitor at least 2 seconds after 0.6 volts is applied

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	5.103	4.75	5.50	PASS

WAVEFORM AND MEASUREMENTS
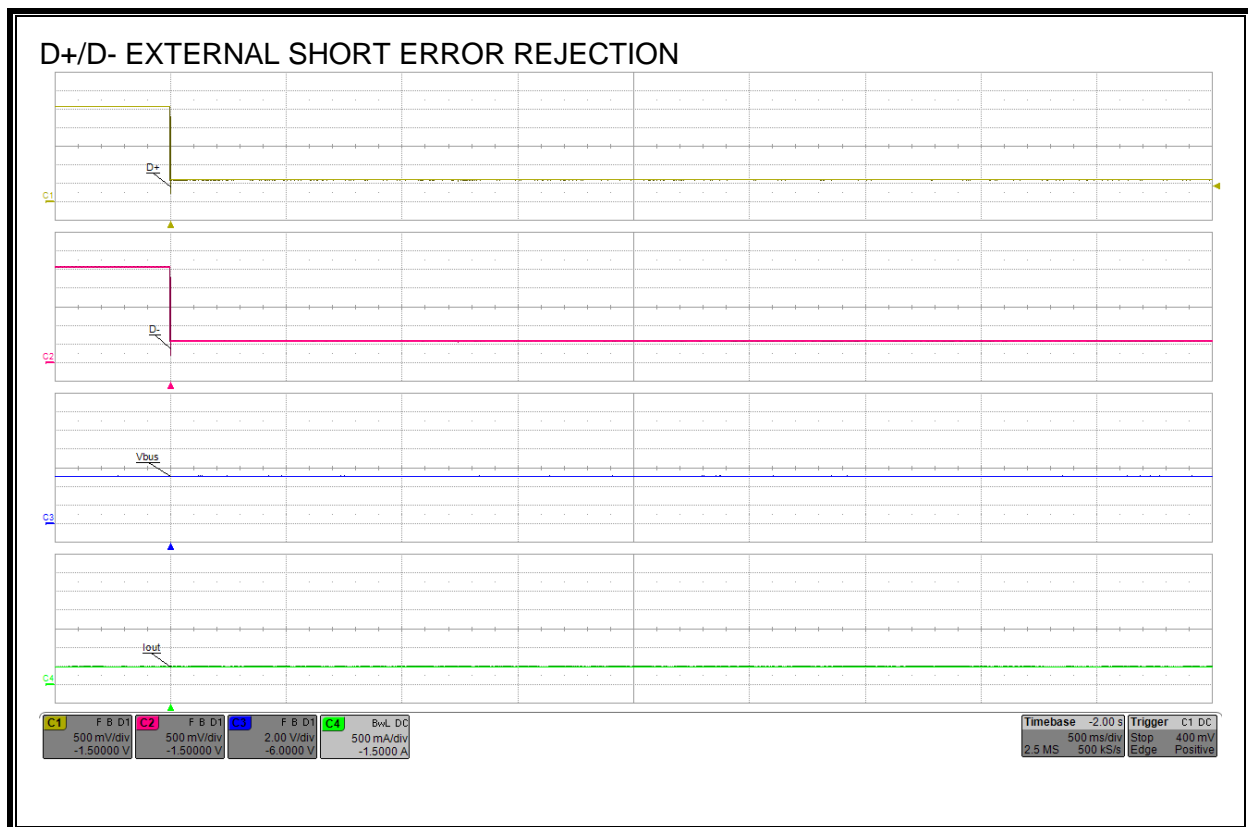
7.5.3. Recovery from D+/D- External Short

LIMITS AND RESULTS

Initial Condition: D+ and D- externally shorted together and held at 0.6 volts
Setup: Short is removed and D- allowed to float
Response: HVCDP asserts Rdm_dwn
Applied Waveform: 0.6 V is applied to D-
Requirement: Vbus makes a normal transition from 5 volts to 12 volts

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 5.5 V (Max Vbus_5v)	39.86	20	60	PASS
Tv_new_request	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 10.8 V (Min Vbus_hv)	40.69		200	PASS

WAVEFORM AND MEASUREMENTS

RECOVERY FROM D+/D- EXTERNAL SHORT
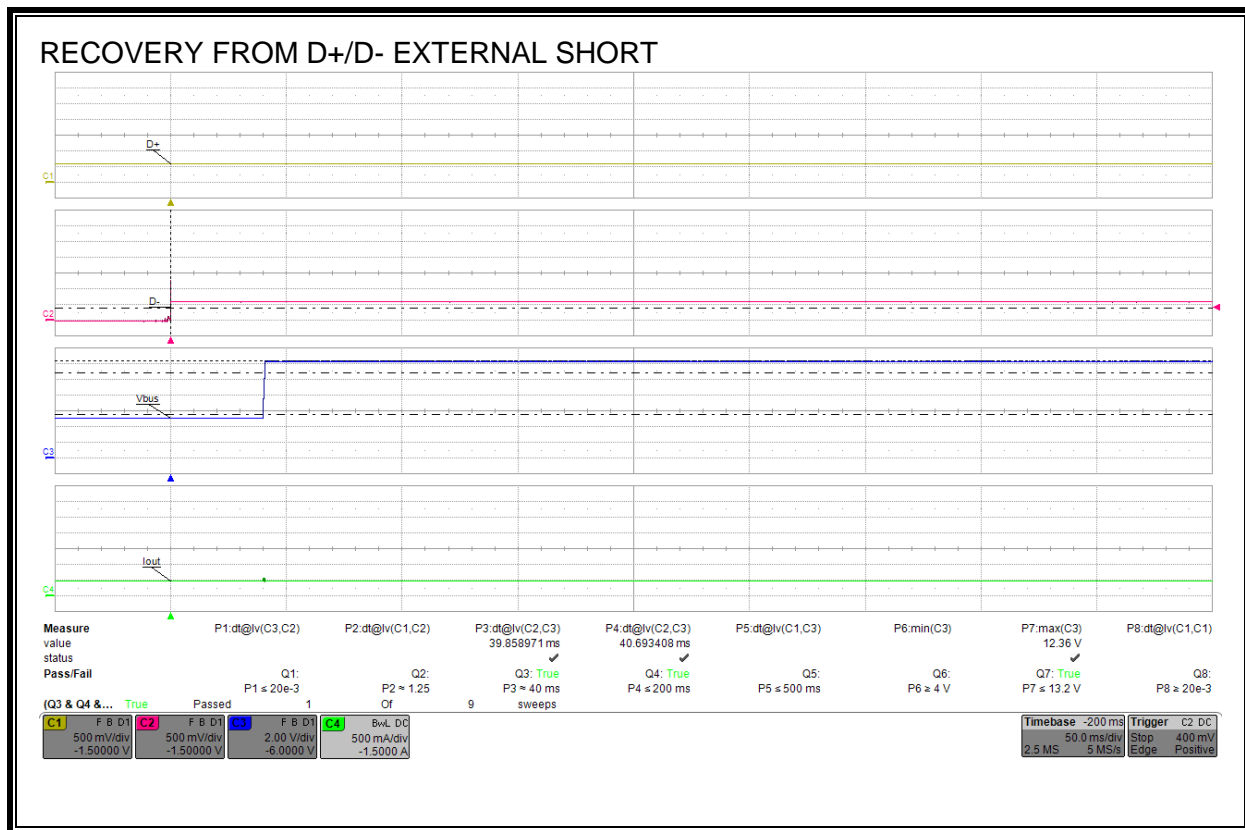
7.6.   Continuous Mode PD Request Recognition

7.6.1. Upper Bound of Tglitch_mode_change

LIMITS AND RESULTS

Charger Transition	Observation of Vbus	Pass/Fail
To Continuous Mode using D+ Pulse	Increments	PASS
To Continuous Mode using D- Pulse	Decrements	PASS

WAVEFORM FOR TRANSITION USING D+

TRANSITION TO CONTINUOUS MODE USING D+

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WAVEFORM FOR TRANSITION USING D-
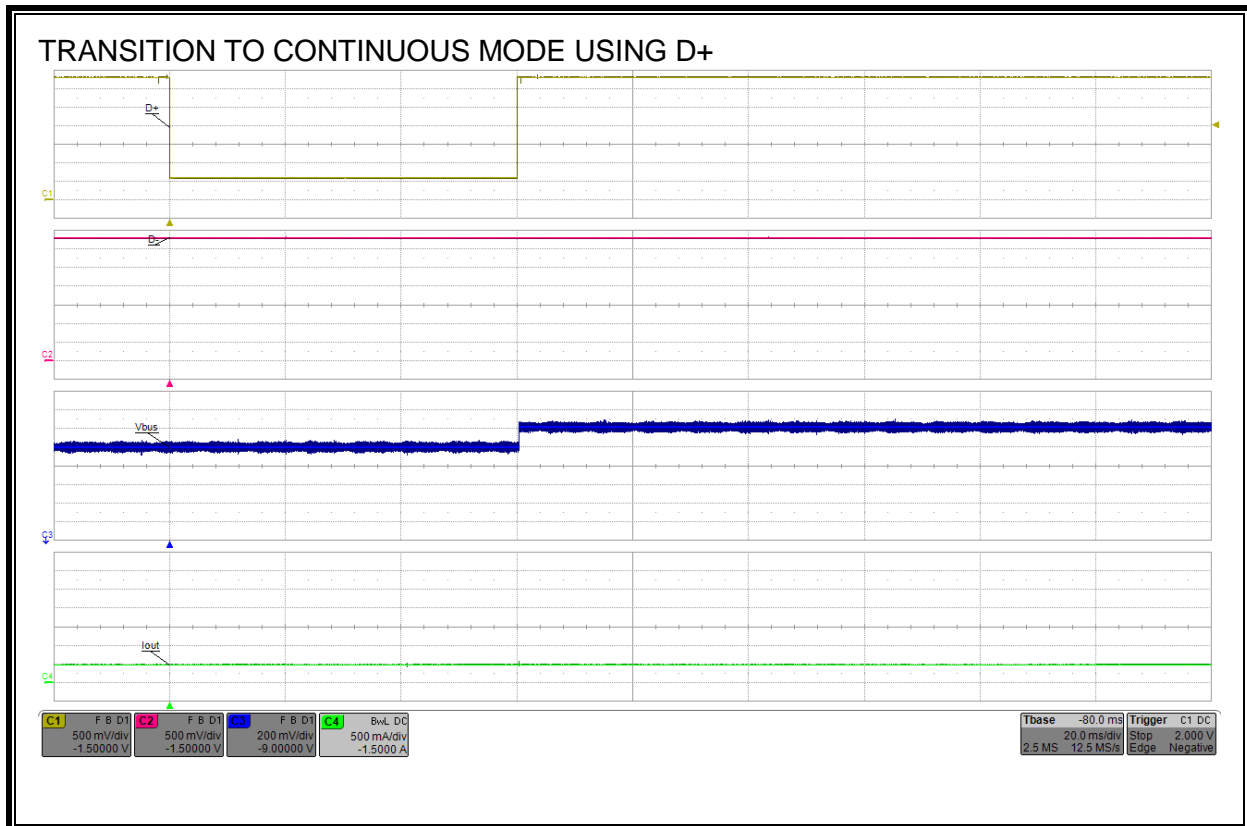
TRANSITION TO CONTINUOUS MODE USING D-
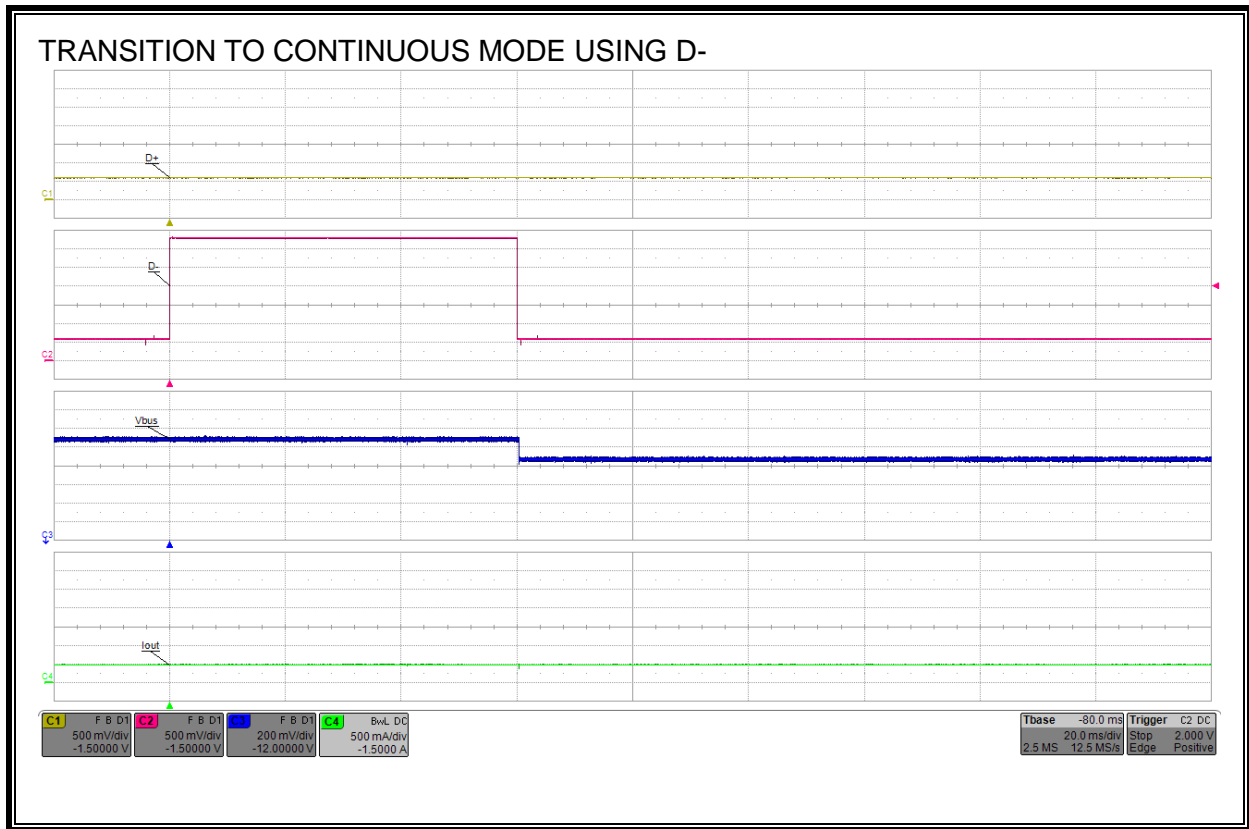
7.6.2. Tv_cont_change & Vbus_cont_step at Upper Bound of D-Tglitch_cont_change

Tv_cont_change LIMITS AND RESULTS

Vbus Transition	Time from leading edge of request to completion of Vbus transition (ms)	Maximum Limit (ms)	Pass/Fail
11.8 V to 11.6 V	0.86	60.0	PASS

Vbus_cont_step LIMITS AND RESULTS

Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
11.8 V to 11.6 V	12.072	11.877	0.195	0.150	0.250	PASS

DECREMENT WAVEFORM
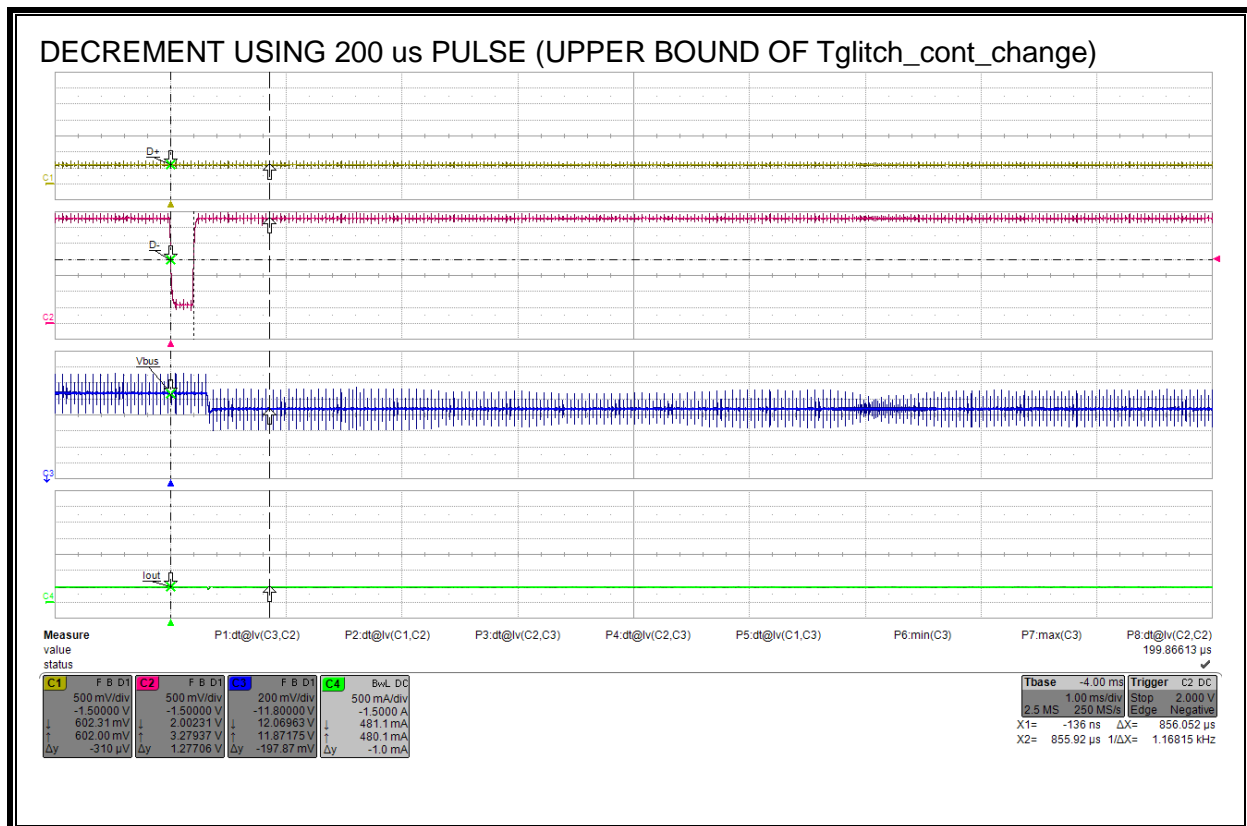
7.6.3. Lower Bound of D- Tglitch_cont_change

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Attempt to Decrement using D- Pulse Width < Minimum Tglitch_cont_change	Vbus does not Change	PASS

WAVEFORMS

RESPONSE USING 100 us PULSE (LOWER BOUND OF Tglitch_cont_change)
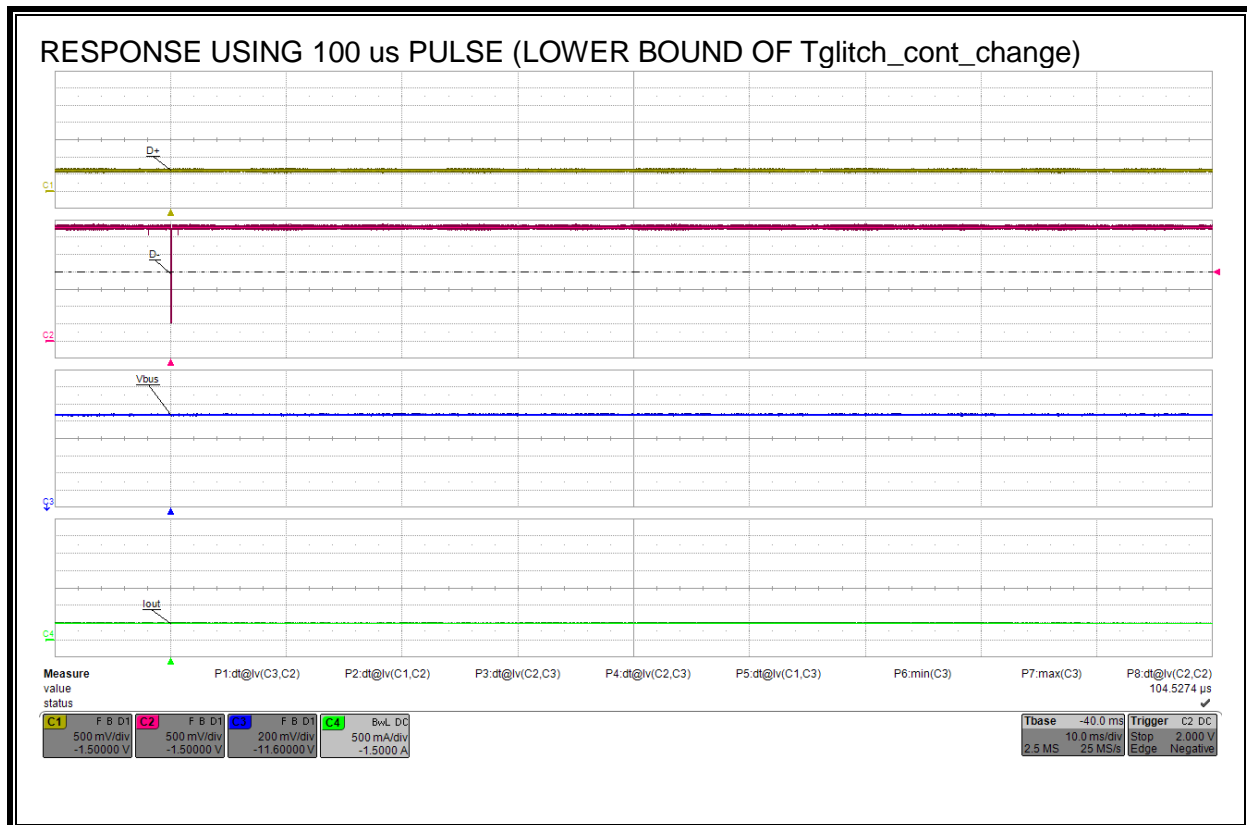
7.6.4. Lower Bound of D- Tinactive

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Two Decrement Pulses with minimum Tinactive timing	Vbus Decrements Twice	PASS

DECREMENT WAVEFORM

TWO DECREMENTS WITH 200 us BETWEEN PULSES (LOWER BOUND OF Tinactive)

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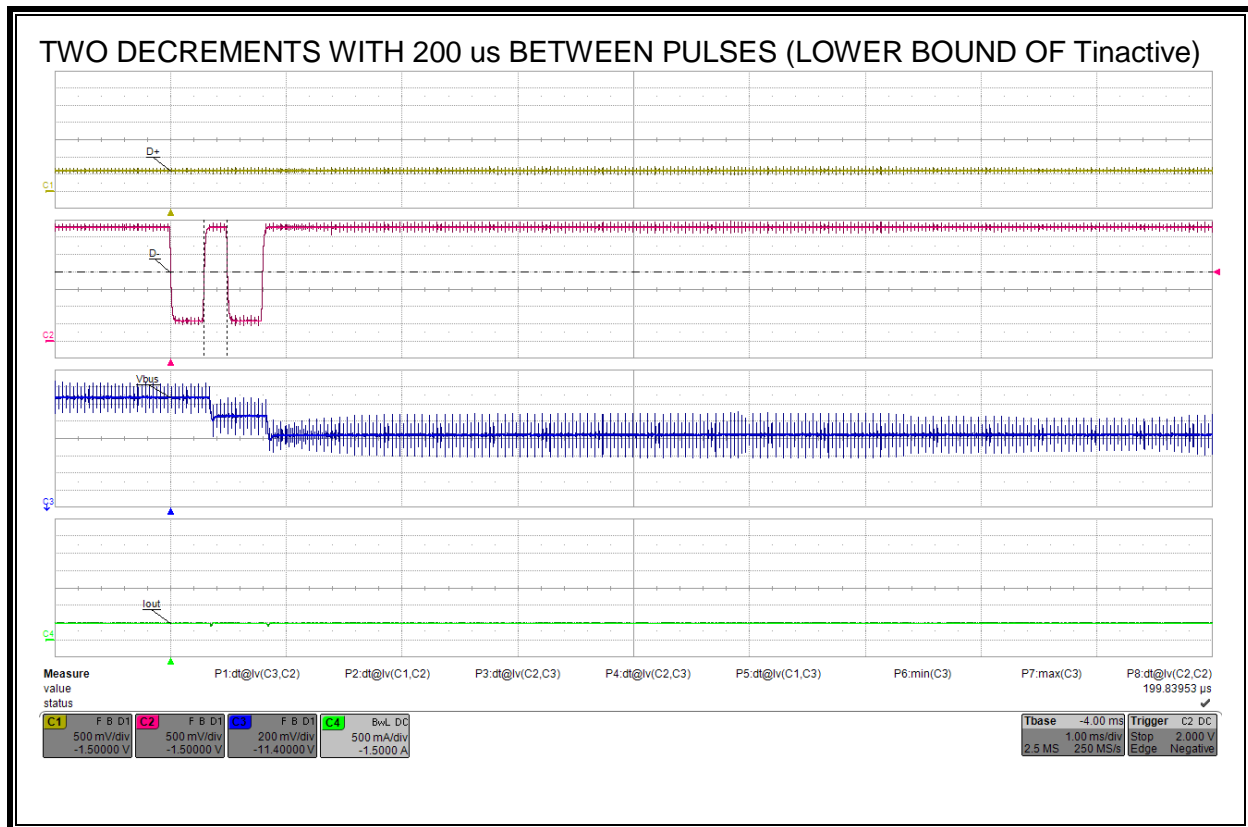
7.6.5. Tv_cont_change & Vbus_cont_step at Upper Bound of D+ Tglitch_cont_change

Tv_cont_change LIMITS AND RESULTS

Vbus Transition	Time from leading edge of request to completion of Vbus transition (ms)	Maximum Limit (ms)	Pass/Fail
5.0 V to 5.2 V	0.86	60.0	PASS

Vbus_cont_step LIMITS AND RESULTS

Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
5.0 V to 5.2 V	5.103	5.314	0.211	0.150	0.250	PASS

INCREMENT WAVEFORM
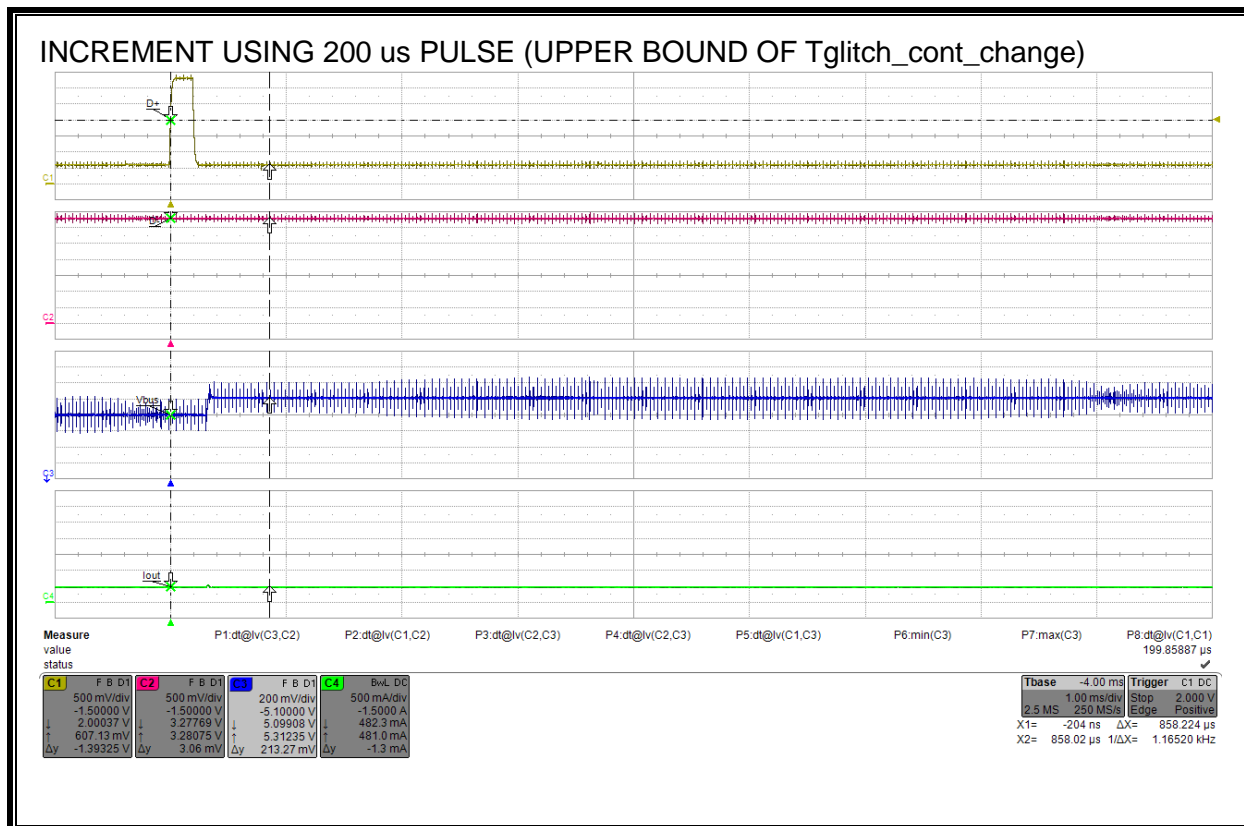
7.6.6. Lower Bound of D+ Tglitch_cont_change

LIMITS AND RESULTS

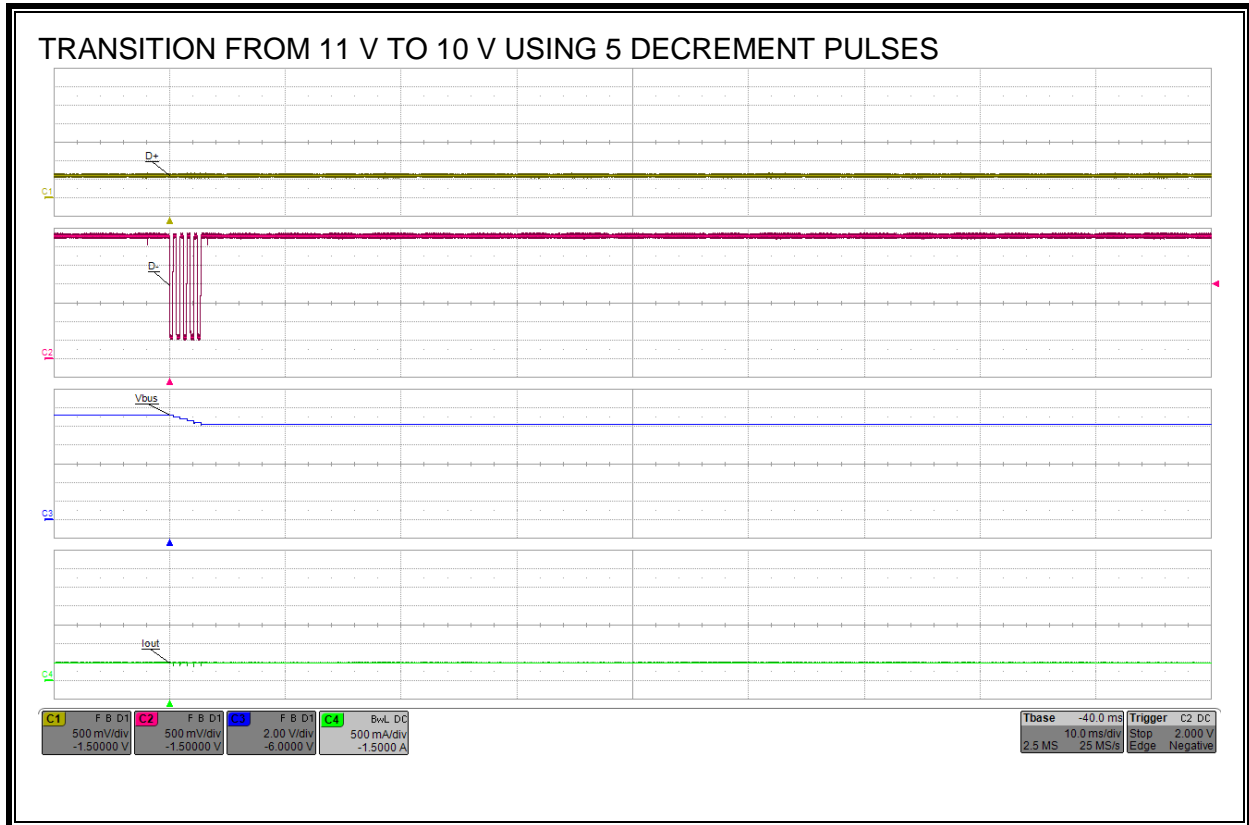| D+ / D- Command	Observation of Vbus	Pass/Fail
Attempt to Increment using D+ Pulse Width < Minimum Tglitch_cont_change	Vbus does not Change	PASS

WAVEFORMS

RESPONSE USING 100 us PULSE (LOWER BOUND OF Tglitch_cont_change)
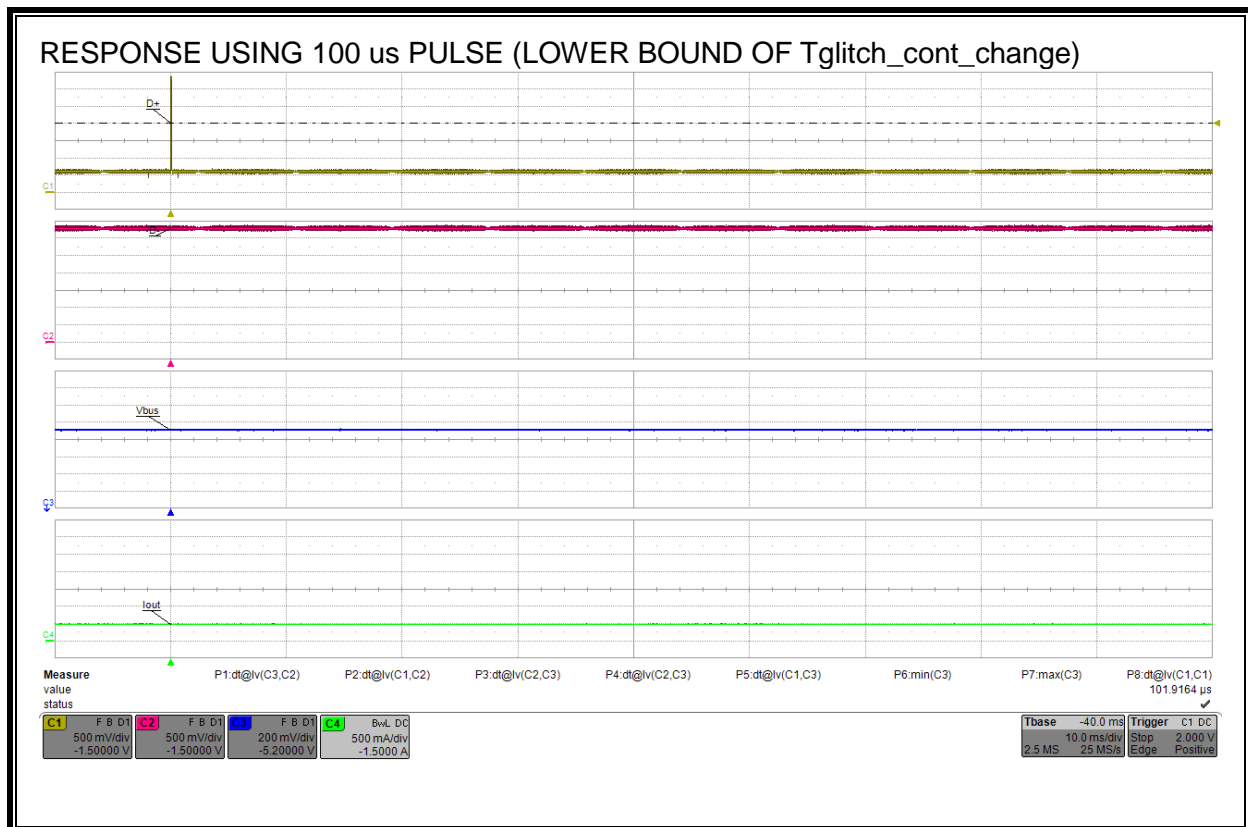
7.6.7. Lower Bound of D+ Tinactive

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Two Increment Pulses with minimum Tinactive timing	Vbus Increments Twice	PASS

INCREMENT WAVEFORM

TWO INCREMENTS WITH 200 us BETWEEN PULSES (LOWER BOUND OF Tinactive)
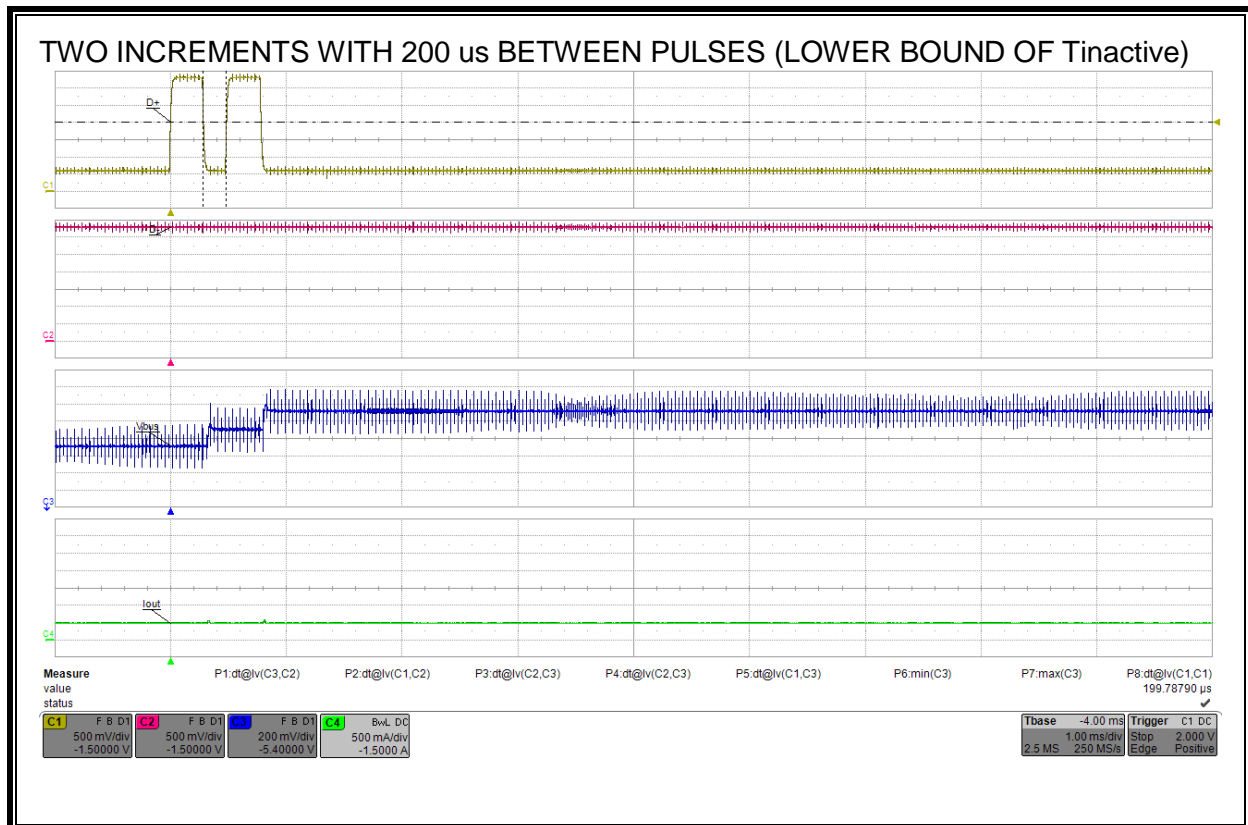
7.6.8. Cumulative Tolerance of Vbus_cont_step

CUMULATIVE Vbus,cont,step LIMITS AND RESULTS

Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
5 V to 11 V	5.10	11.24	6.14	4.50	7.50	PASS
11 V to 10 V	11.24	10.23	1.01	0.75	1.25	PASS

Vbus Transition	Observation of Vbus	Pass/Fail
5 V to 11 V	Vbus does not decrement during the process	PASS
11 V to 10 V	Vbus does not increment during the process	PASS

INCREMENT WAVEFORM

TRANSITION FROM 5 V TO 11 V USING 30 INCREMENT PULSES

DECREMENT WAVEFORM

TRANSITION FROM 11 V TO 10 V USING 5 DECREMENT PULSES
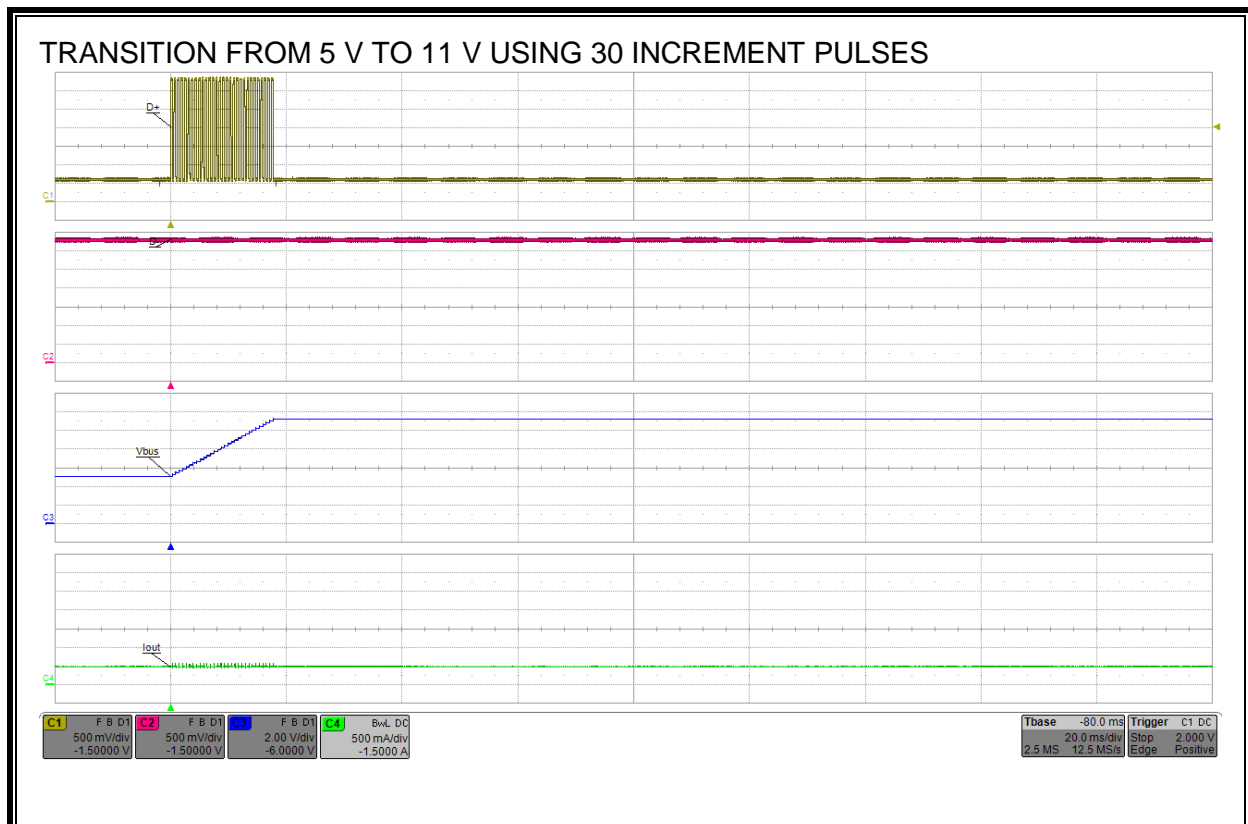
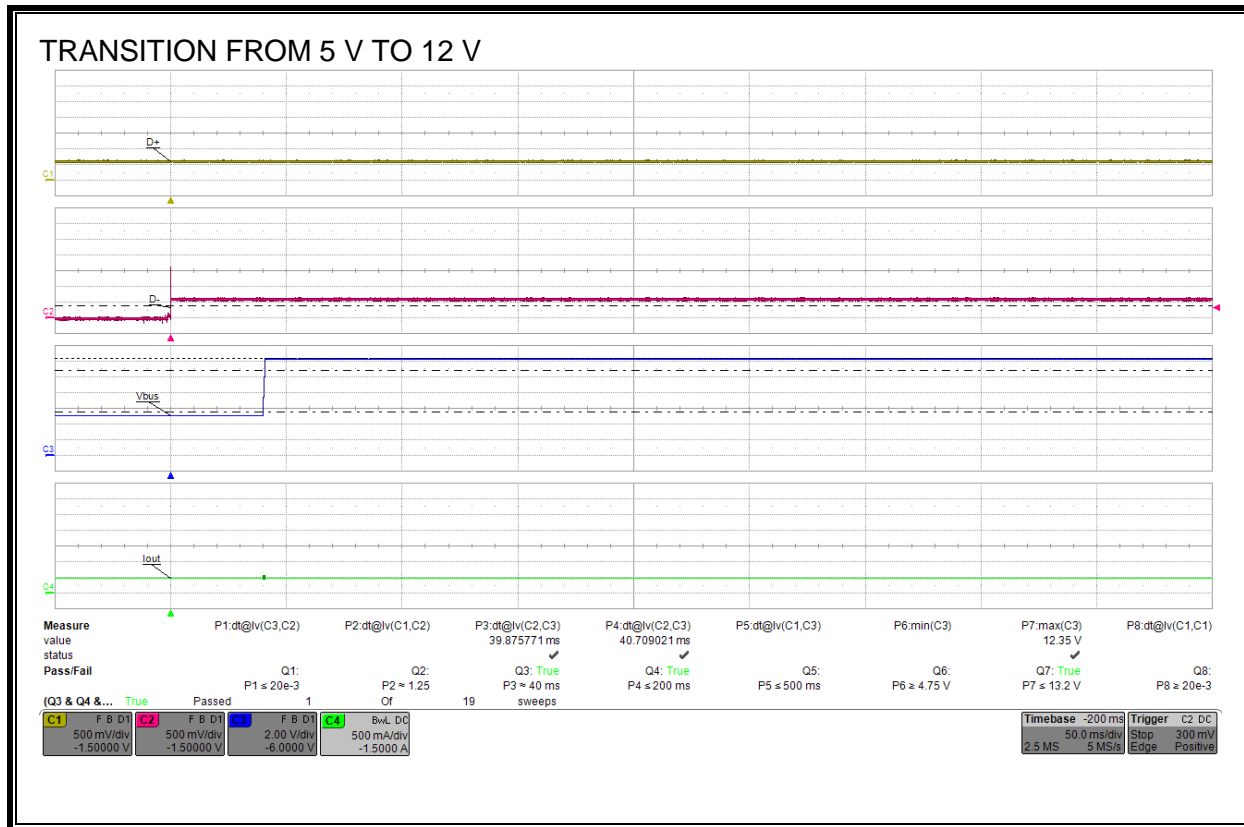## 7.7. Transition from Continuous Mode to Fixed Mode

7.7.1. Transition from 10 V to 5 V

LIMITS AND RESULTS

| Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 9.1 V (Min Vbus_hv)	41.25	20	60	PASS
Tv_new_request	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 5.5 V (Max Vbus_5v)	41.82		200	PASS

WAVEFORM AND MEASUREMENTS
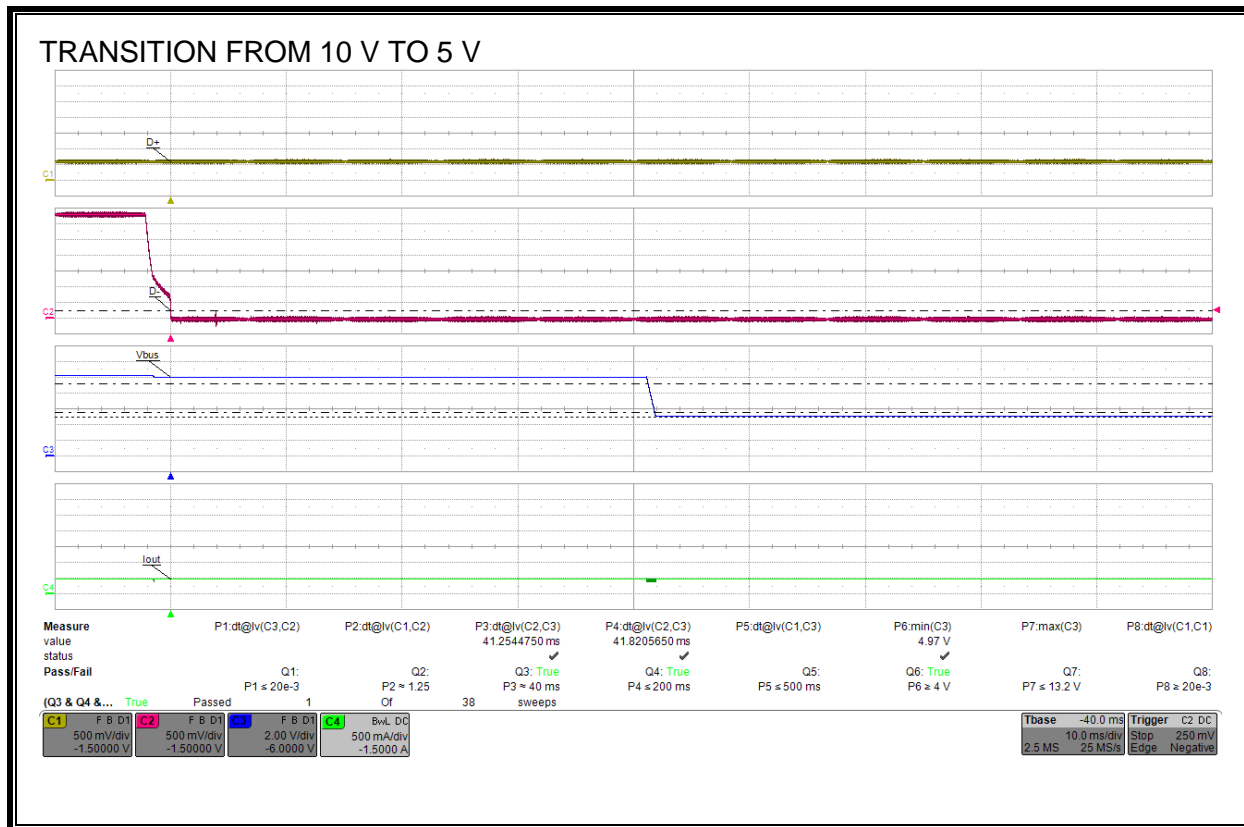
7.7.2. Transition from 5 V to 12 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 5.5 V (Max Vbus_5v)	39.88	20	60	PASS
Tv_new_request	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 10.8 V (Min Vbus_hv)	40.71		200	PASS

WAVEFORM AND MEASUREMENTS

TRANSITION FROM 5 V TO 12 V

UL TAIWAN CO., LTD.   FORM NO: CCSUP4701J
1ST FL, 260 DA-YEH ROAD, PEITOU, TAIPEI CITY, 112 TAIWAN   TEL: +886.2.7737.3000
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7.7.3. Transition from 12 V to 9 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 10.8 V (Min Vbus_hv)	41.36	20	60	PASS
Tv_new_request	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 9.9 V (Max Vbus_hv)	41.51		200	PASS

WAVEFORM AND MEASUREMENTS

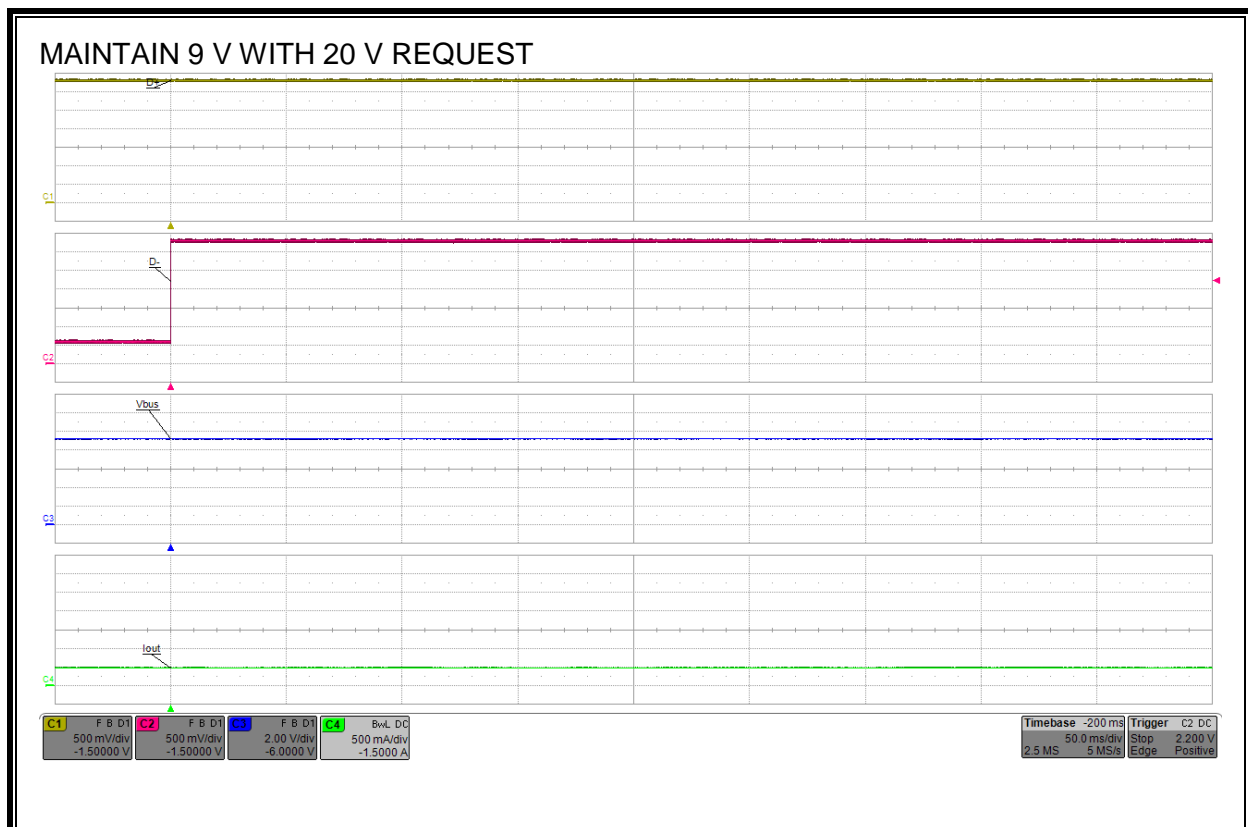TRANSITION FROM 12 V TO 9 V
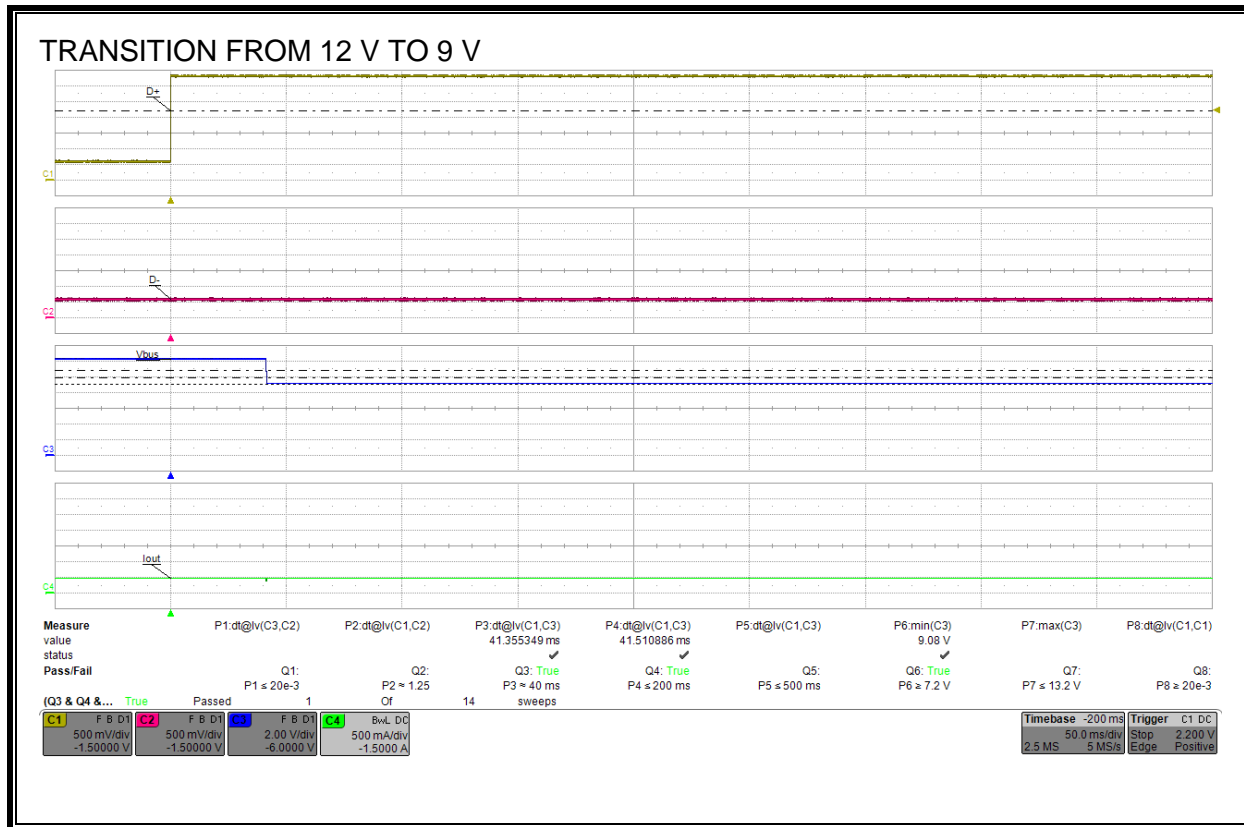
7.7.4. Maintain 9 V with 20 V Request

LIMITS AND RESULTS

Initial Condition: Vbus is 9 volts

Observation Period: Monitor for longer than 200 ms (Max Tv_new_request) after 20 Volt Request is asserted

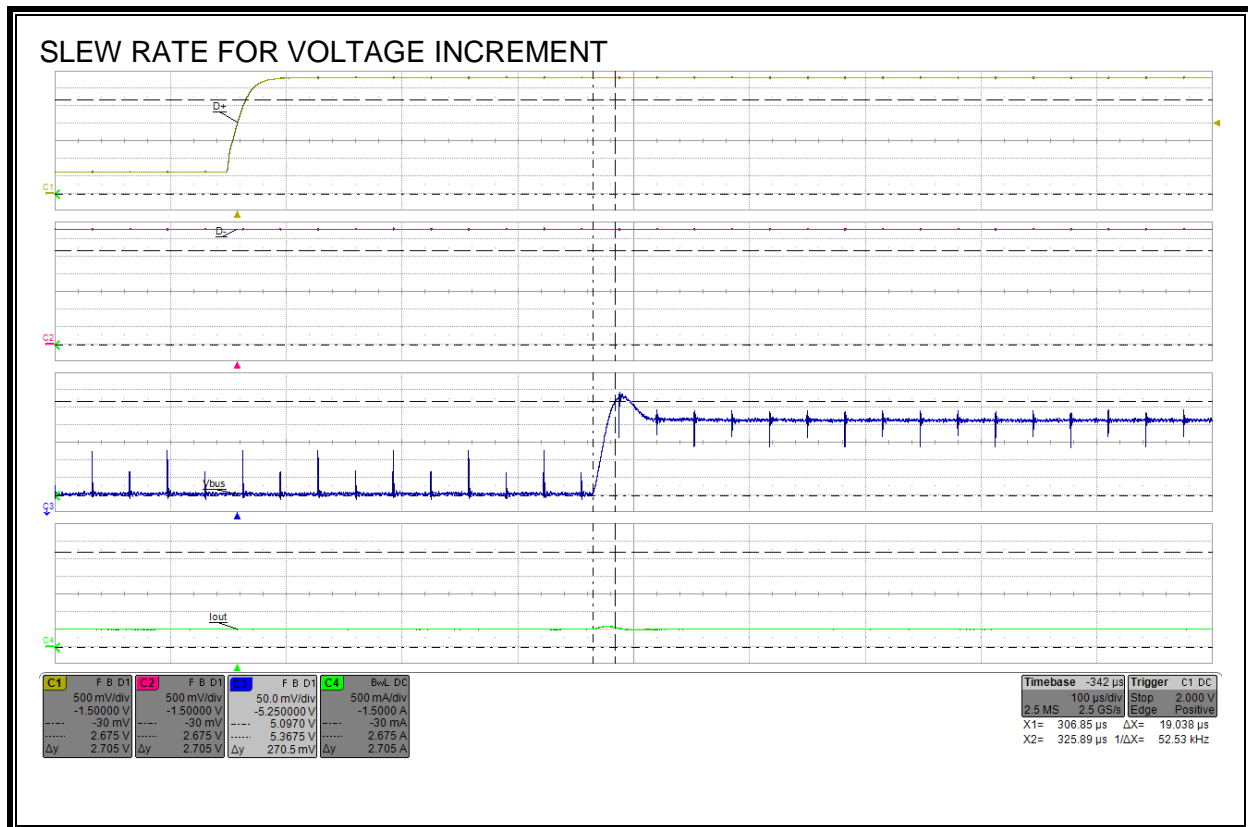| Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	9.203	8.10	9.90	PASS

WAVEFORM AND MEASUREMENTS

7.8.   Operating Characteristics
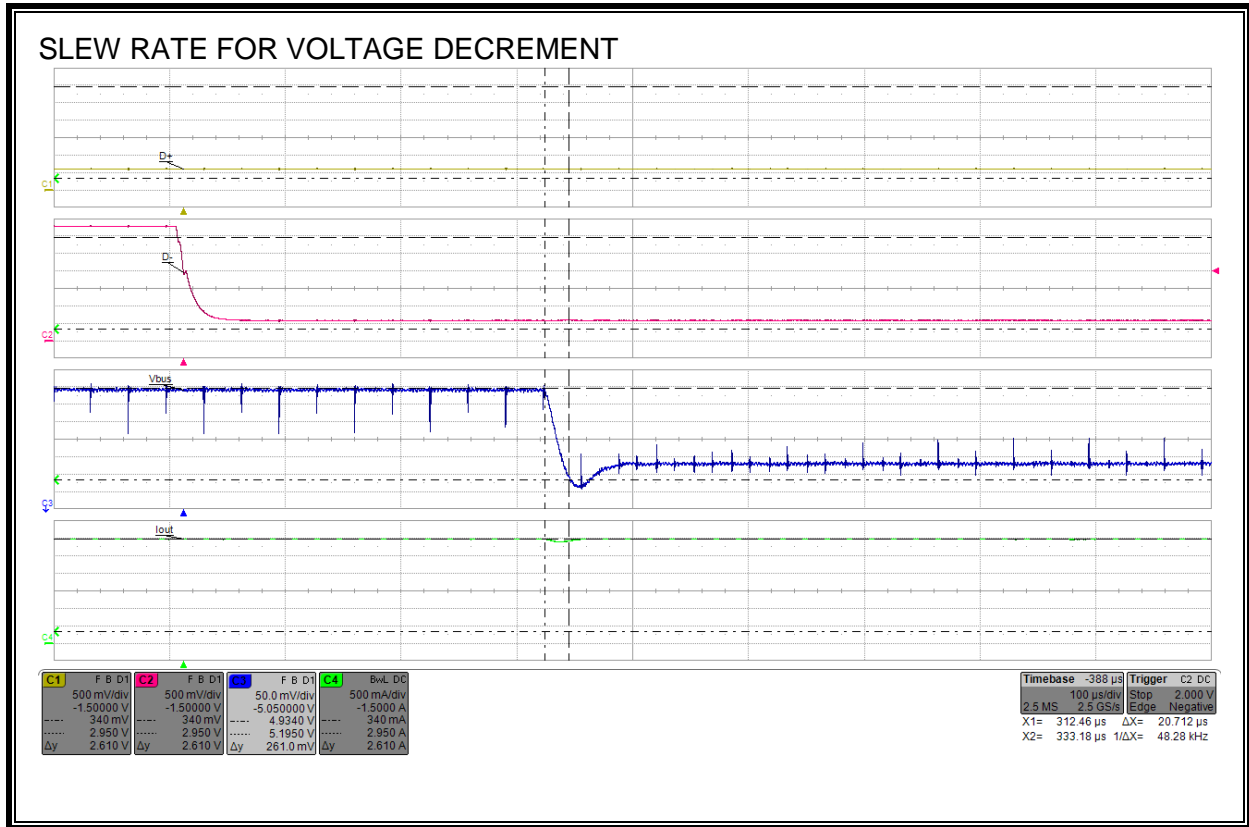
7.8.1. Vslew_max

Vslew_max LIMITS AND RESULTS

Vbus Transition	Delta Voltage (mV)	Delta Time (usec)	Slew Rate (mV/usec)	Maximum Limit (mV/usec)	Pass/Fail
5.0 V to 5.2 V with 500 mA Load	270.50	19.00	14.237	30	PASS
5.2 V to 5.0 V with 3 A Load	261.00	20.70	12.609	30	PASS

WAVEFORM FOR INCREMENTING SLEW RATE

SLEW RATE FOR VOLTAGE INCREMENT

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WAVEFORM FOR DECREMENTING SLEW RATE

SLEW RATE FOR VOLTAGE DECREMENT

7.8.2. Minimum Vbus_cont_range

Minimum Vbus_cont_range LIMITS AND RESULTS

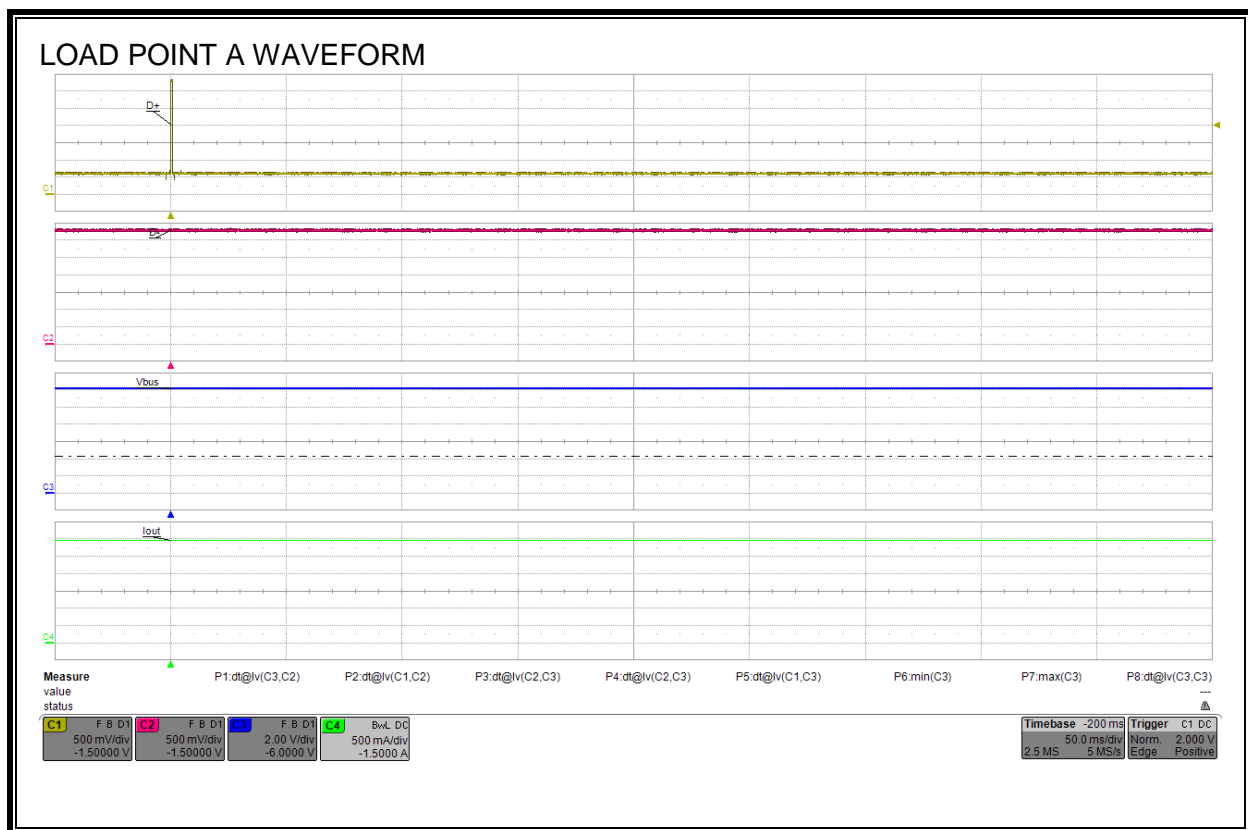| Condition	Measured Value (V)	Minimum Limit (V)	Pass/Fail (Measured value must be <= Minimum Limit)
Current = 0.2 A	3.687	3.80	PASS
Current = Max Rated (3 A)	3.547		

7.9. Power Profile
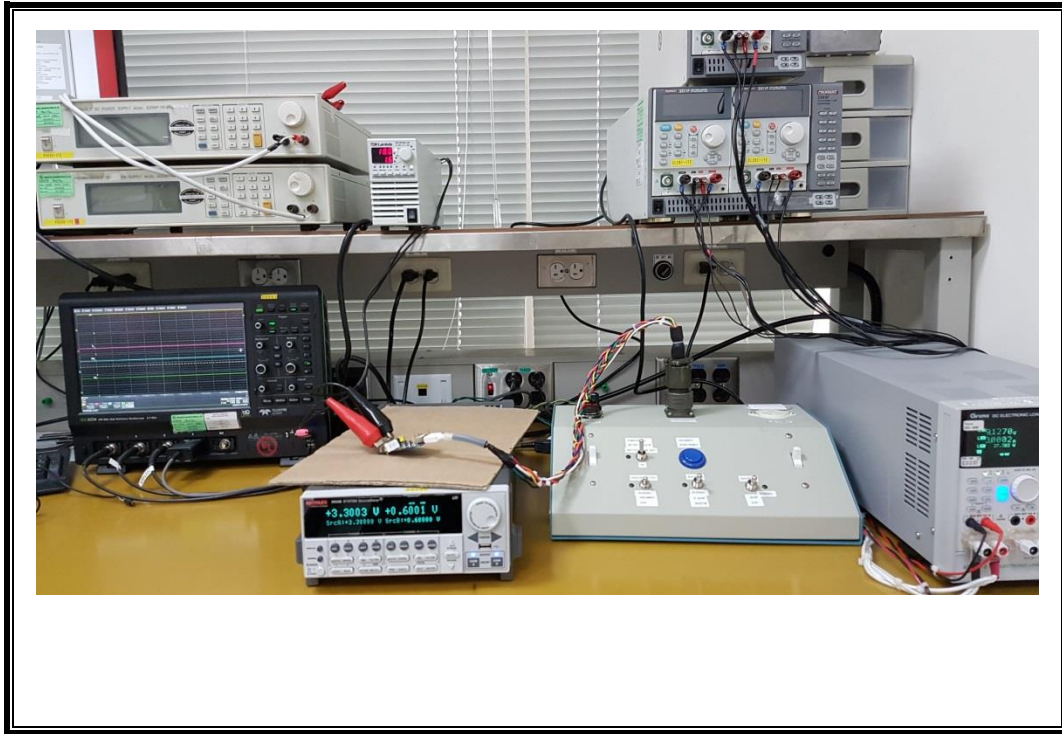
7.9.1. Load Point A & Minimum Pmax

LOAD POINT A LIMITS AND RESULTS

Measured Current (A)	Measured Load Point A Voltage Via Increment (V)	Minimum Voltage Limit (V)	Pass/Fail	Pmax (Watts)
3.00	12.210	6.00	PASS	36.63

VBUS REACHES LOAD POINT A

LOAD POINT A WAVEFORM

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8. SETUP PHOTO

END OF REPORT